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Project Information

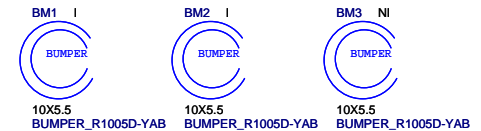
Phase: PVT 2011/07/19
SCH: P2-H67 V0.1
SVID: 103C
SSID: 17A1

BIOS Licence Label

LBL1
BIOS_LICENCE
Note:
AMI uEFI

PCB Fab Note

PCB1
Printed Circuit Board
PC BOARD
CRITICAL
4-Layer PCB, Color Green Soldermask, White Silkscreen, 9.6X9.3 inch, Rev:1.00, ROHS
010162P02-GL7-G



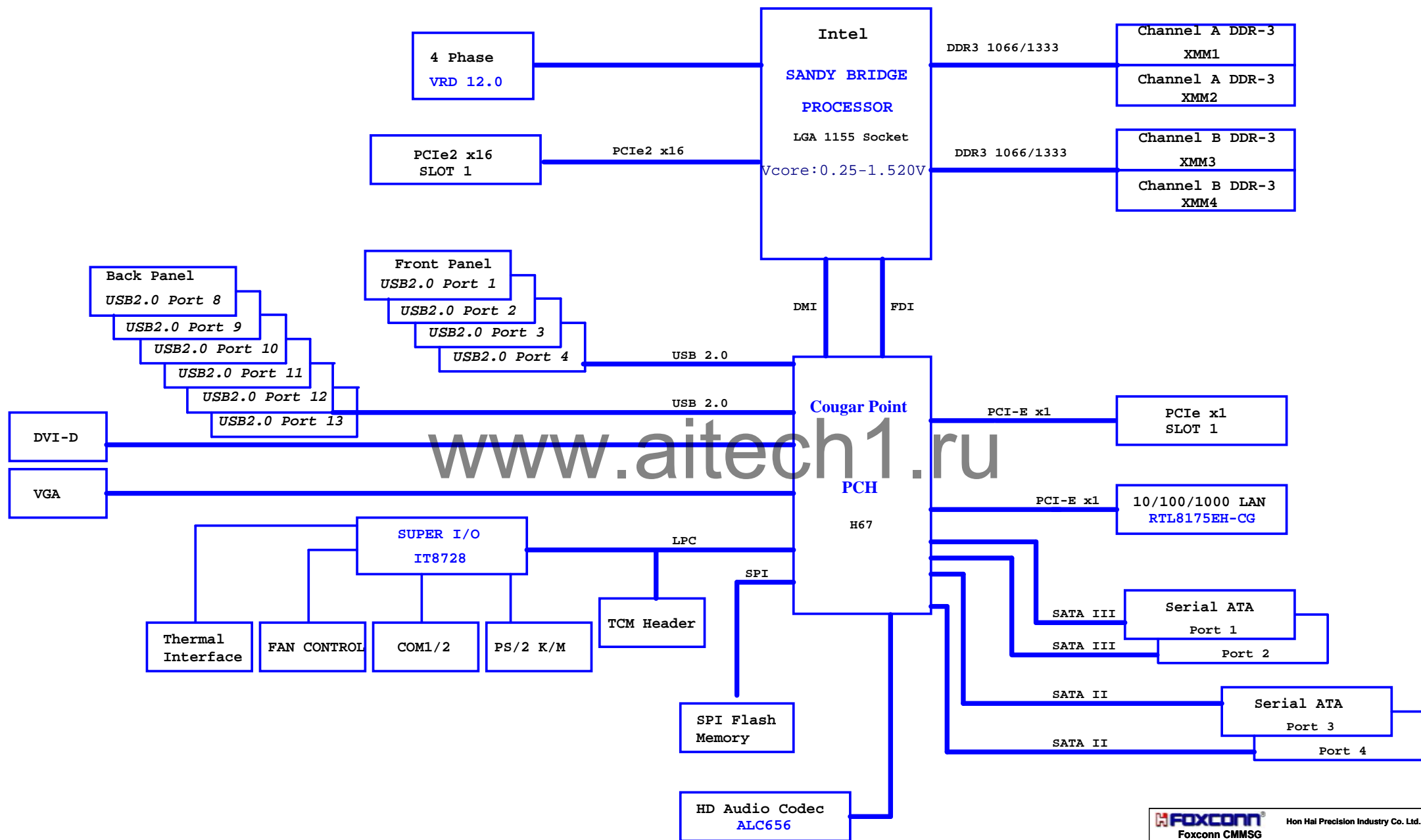
4 LAYER			1080
Description		COPPER(Oz)	Thickness(MILS)
L1-Top Signal Layer		.5(Before Plating)	1.9(+0.8/-0.8)
Prepreg			2.7(+0.8/-0.4)
L2-Inner1 Layer		1	1.2(+/-10%)
CORE	Fab Vender will adjust Core thickness to achieve overall board		47(REF)-OPEN
L3-Inner 2 Layer		1	1.2(+/-10%)
Prepreg			2.7(+0.8/-0.4)
L4-Bottom Signal Layer		.5(Before Plating)	1.9(+0.8/-0.8)

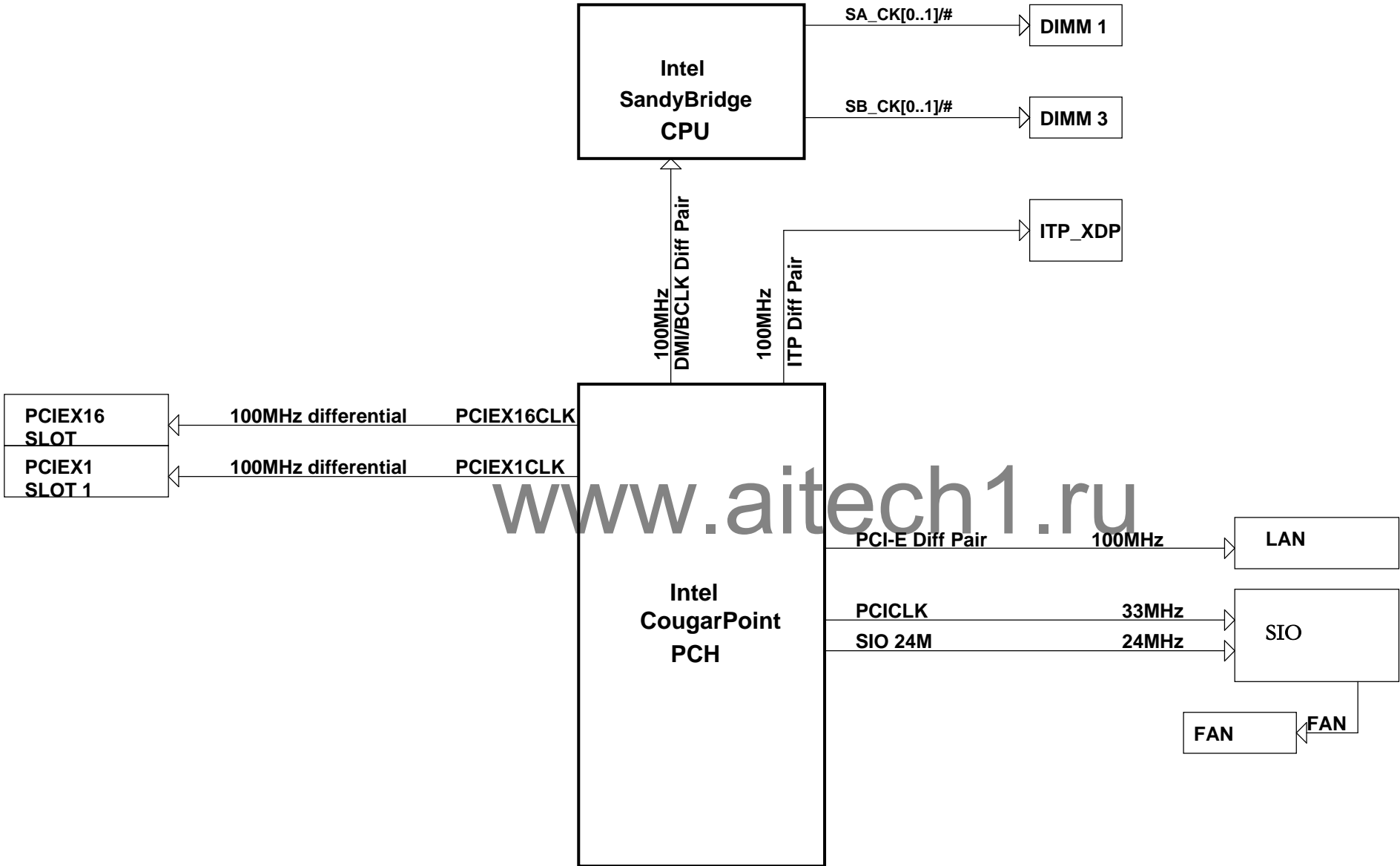
PAGE	TITLE
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03	CLOCKS DIAGRAM
04	POWER DISTRIBUTION DIAGRAM
05	POWER FLOW DIAGRAM
06	POWER GOOD DIAGRAM
07	POWER SEQUENCE DIAGRAM
08	BLANK
09	XDP & DMI DEBUG
10	MCP-CLK/ CTRL/ MISC/DEBUG
11	MCP- DDR3 CHANNEL A & B
12	MCP- PCIE/ DMI/ FDI
13	MCP-VCC/VDDDQ/VCCIO/VCCCP
14	MCP- VCCAXG/VSS
15	PCH DEBUG PORT
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17	DDR3CHADIMM0 - XMM2 Blue
18	DDR3CHBDIMM0 - XMM3 Black
19	DDR3CHBDIMM0 - XMM2 Blue
20	PCH - DMI/ PCIE/ USB
21	PCH - PCI
22	PCH - SATA/ MLINK/ GPIO
23	PCH - GPIO/SMBUS/MISC
24	PCH - DP/ FDI/ VGA/ CLOCK
25	PCH - POWER & GND
26	PCH-PLL FILTER & DCPING
27	PCIE_x16
28	PCIE_x1
29	TCM
30	VGA
31	DVI
32	USB POWER
33	AUDIO CODEC
34	AUDIO CONN/ INT SPKR
35	PCI Slot
36	RTL8171EH-CG
37	RJ45_USB 2.0 CONN
38	REAR USB
39	FRONT USB
40	SATA CONN / BUZZER

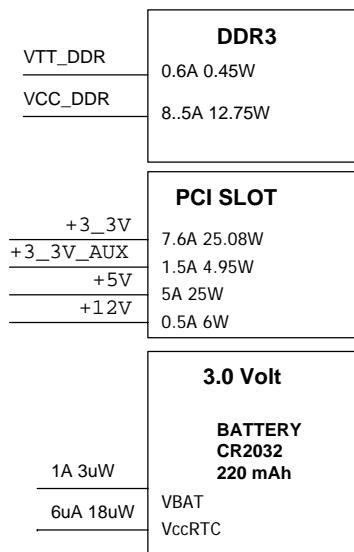
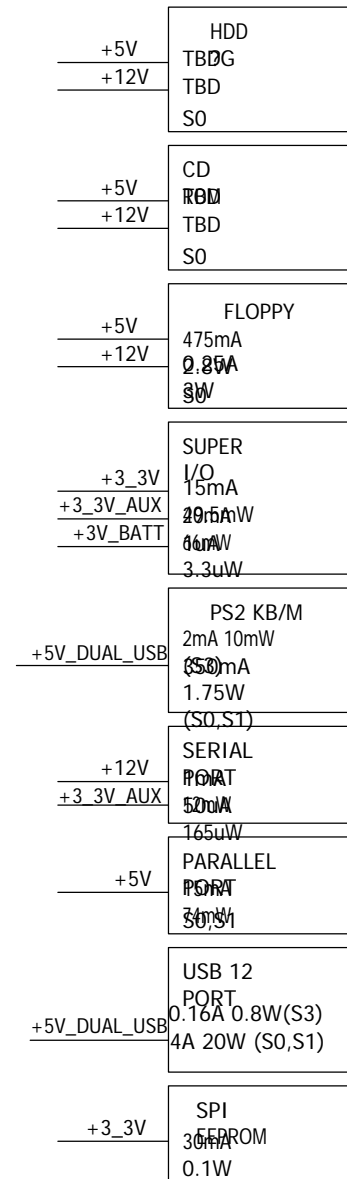
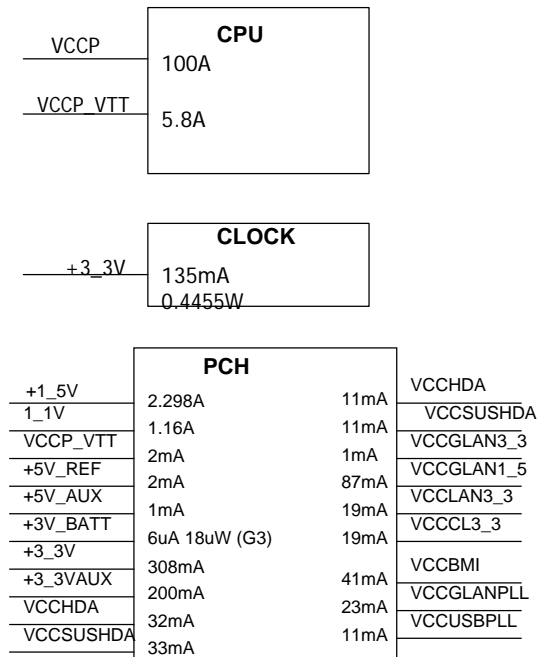
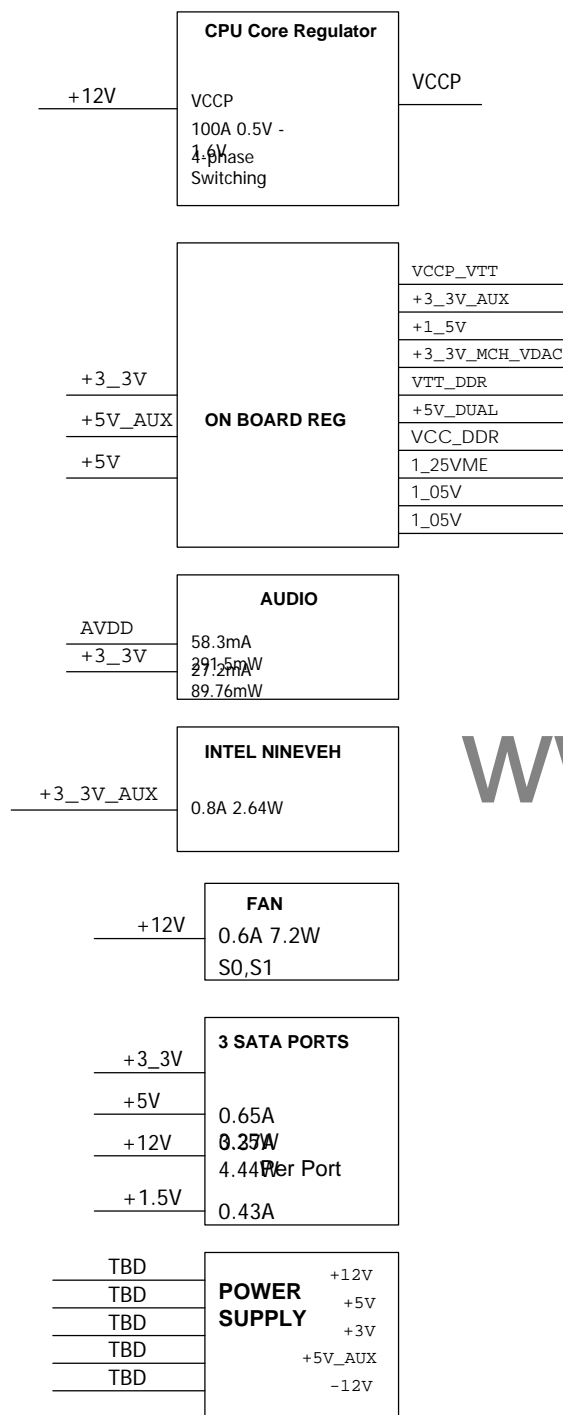
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42	PS2 Connector
43	LPT and SERIAL
44	IT8893E
45	SPI EEPROM & LPC Debug
46	FRONT PANEL & DSW
47	LED / HEADER
48	FAN HEADERS
49	POWER INPUT & EMI CAP
50	+5V_DUAL
51	+3P3V_AUX
52	+1P8V_SFR&+1P1V_DUAL
53	+1P05V
54	VCC_DDR/ VTT_DDR
55	VCORE
56	VCORE PHASE 1 & 2
57	VCORE PHASE 3
58	+VCC_AXG
59	VCCIO
60	VCCSA
61	EUP&+LPS
62	Dummy Load
63	PCH GPIO Information
64	SIO/Others GPIO Information
65	Strapping Information
66	CHANGE LIST

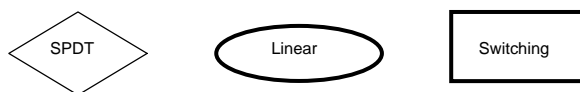
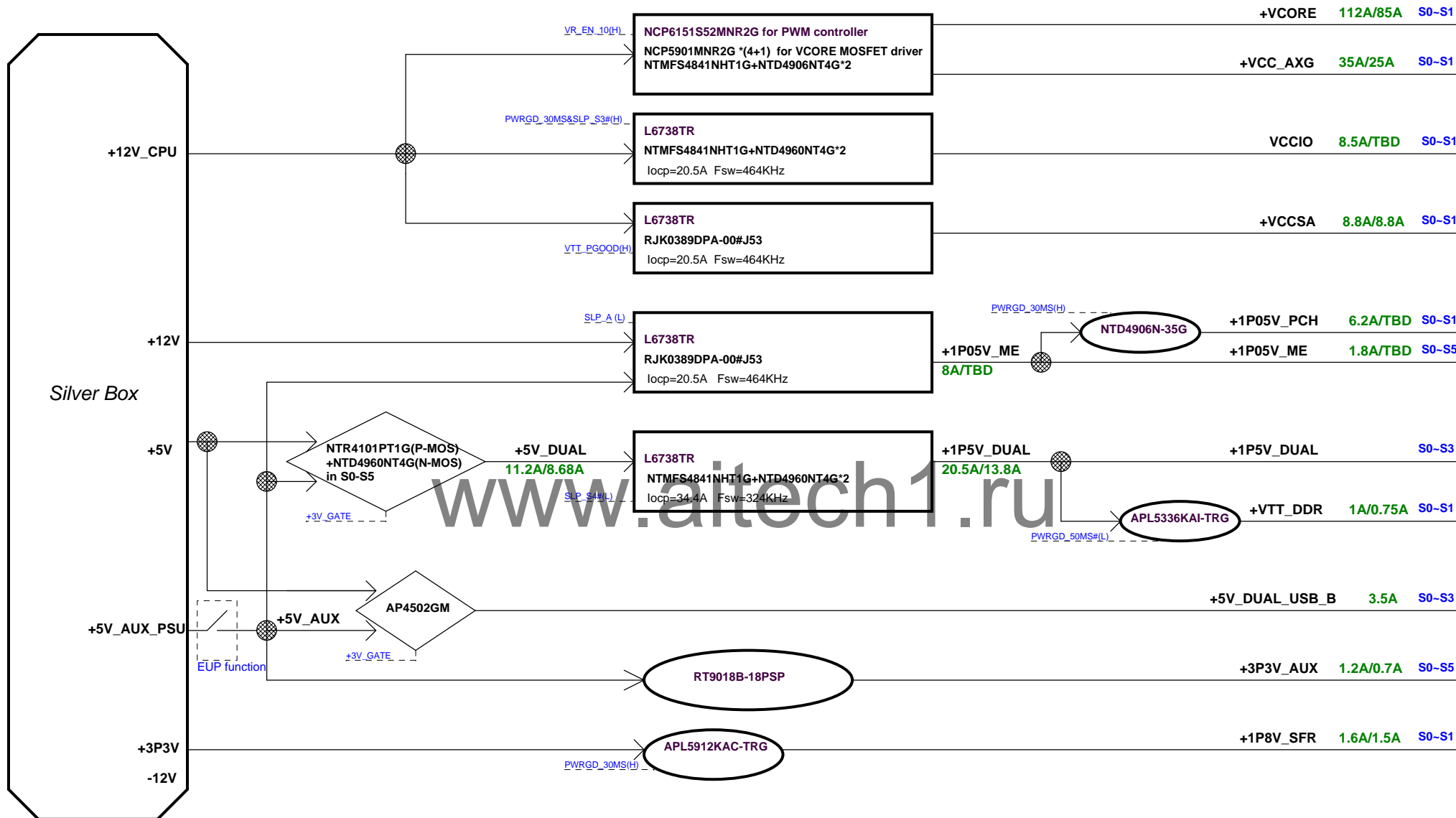
Program Phase	PCB Revision	Color of PCB	Silkscreen
EVT1		RED	YELLOW
EVT2		RED	WHITE
DVT1	REV 0.10	BLUE	YELLOW
DVT2	REV 0.20	BLUE	WHITE
PVT/MVB/MP	REV 1.00	GREEN	WHITE

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Title TOC / SCH INDEX			
Size Custom	Document Number Magellan-H67		Rev 0.1
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Power Rail


Control signal

Note:
xxA/ooA mean I_{max} / I_{tdc}

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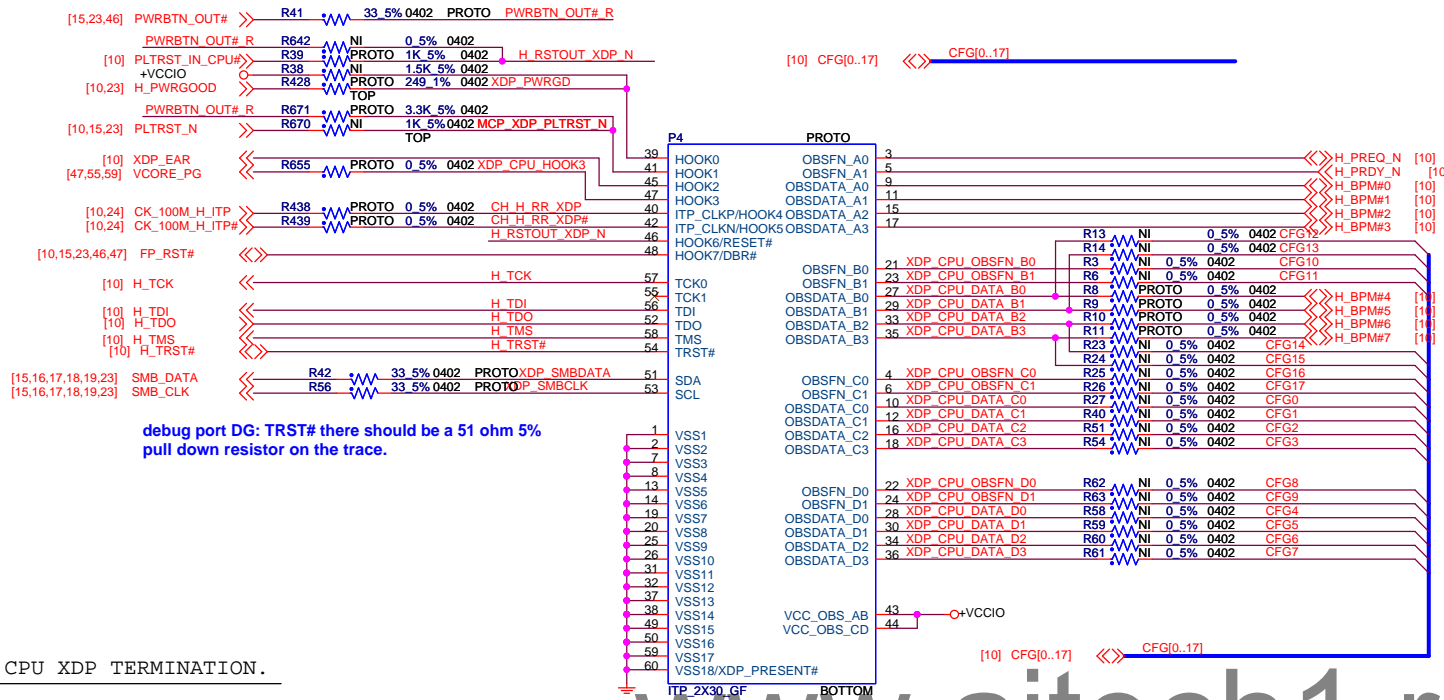
		Hon Hai Precision Industry Co. Ltd.	
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TEL: 886-2-8076-1055		FAX: 886-2-7075-7301	
Title			
POWER SEQUENCE DIAGRAM			
Size	Document Number		Rev
Custom	Magellan-H67		0.1
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Title			
BLANK			
Size	Document Number		Rev
Custom	Magellan-H67		0.1
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Close Branch

Intel MCP XDP Debugging Connector



CPU XDP TERMINATION.

BPM#0[0..5] : the length accounts for both the distance from the CPU to XDP connector and the sub to the termination should less than 1.5".

PLACE TMS/TDI TERMINATION NEAR CPU WITHIN 1.5" OF CPU.

PLACE TDO TERMINATION NEAR CONNECTOR.

PLACE TCK TERMINATION NEAR CPU WITHIN 1.5" OF CPU.

PLACE TRST# TERMINATION ANYWHERE ON ROUTE.

XTP CAD NOTES:

- Place XP port 2 to 4 inches from processor in solder side.
- Match Impedance of the BPM signals to 50 ohm and trace width to 5 mils with 10 mil spacing.
- TCK signal spacing should be 5 mil trace and 10 mil spacing. TCK should split at the XTP and route to CPU.
- FBO signal spacing should be 5 mil trace and 10 mil spacing. Match FBO length to the length of BPM segment from XTP to CPU.
- TMS# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain with pull-up at XTP port.
- TRST# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain startinf from XTP to CPU.
- CPU_RST# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain starting from GMCH to CPU.
- TDI, TDO signal spacing should be 5 mil trace and 10 mil spacing.
- Other signals should have 5 mil trace and 10 mil spacing.

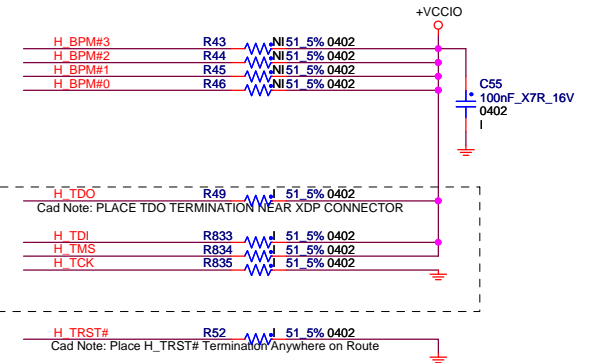
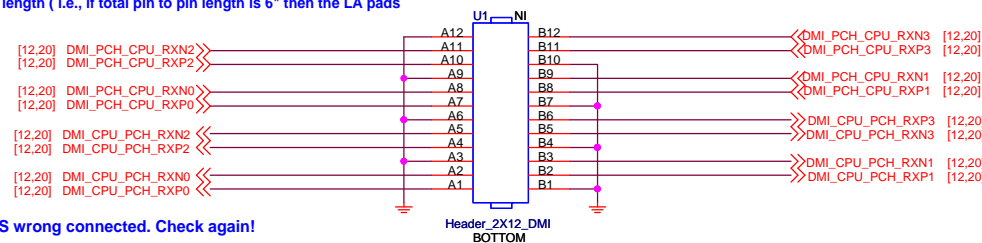


Table 3-1. Processor XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0	PREQ#	I/O	processor 4	4	OBSFN_C0	CFG[16]	I/O	Processor
5	OBSFN_A1	PRDY#	I/O	processor 6	5	OBSFN_C1	CFG[17]	I/O	Processor
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	BPM#[0]	I/O	processor 10	10	OBSDATA_C0	CFG[0]	I/O	Processor
11	OBSDATA_A1	BPM#[1]	I/O	processor 12	12	OBSDATA_C1	CFG[1]	I/O	Processor
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	BPM#[2]	I/O	processor 16	16	OBSDATA_C2	CFG[2]	I/O	Processor
17	OBSDATA_A3	BPM#[3]	I/O	processor 18	18	OBSDATA_C3	CFG[3]	I/O	Processor
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	CFG[10]	I/O	Processor 22	22	OBSFN_D0	CFG[8]	I/O	Processor
23	OBSFN_B1	CFG[11]	I/O	Processor 24	24	OBSFN_D1	CFG[9]	I/O	Processor
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	BPM#[4] / CFG[12]	I/O	processor 28	28	OBSDATA_D0	CFG[4]	I/O	Processor
29	OBSDATA_B1	BPM#[5] / CFG[13]	I/O	processor 30	30	OBSDATA_D1	CFG[5]	I/O	Processor
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	BPM#[6] / CFG[14]	I/O	processor 34	34	OBSDATA_D2	CFG[6]	I/O	Processor
35	OBSDATA_B3	BPM#[7] / CFG[15]	I/O	processor 36	36	OBSDATA_D3	CFG[7]	I/O	Processor
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	PWRGOOD	I	system 40	40	ITPCLK/HOOK4	BCLK_ITP	I	processor
41	HOOK1	BIP_PWRGD_RST#	O	system 42	42	ITPCLK#/HOOK3	BCLK_ITP#	I	processor
43	VCC_OBS_AB	VCCP Voltage of the processor	I		44	VCC_OBS_CD	VCCP Voltage of the processor	I	
45	HOOK2	CFG[0]	O	processor 46	46	HOOK6/RESET#	RESET#	I	processor
47	HOOK3	VR_READY/ SYS_PWROK	O	System 48	48	HOOK7/DBR#	DBR#	O	processor
49	GND	GND	NA		50	GND	GND	NA	
51	SDA ¹	SDA	I/O	system 52	52	TDO	TDO	I	processor
53	SCL ¹	SCL	I/O	system 54	54	TRSTn	TRST#	O	processor
55	TCK1	Open	NA		56	TDI	TDI	O	processor
57	TCK0	TCK	O	processor 58	58	TMS	TMS	O	processor
59	GND	GND	NA		60	GND	GND (or XDP_PRESEN T# if required)	NA	

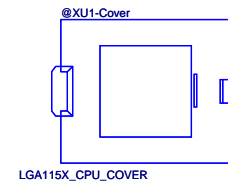
Intel DMI Debug Connector



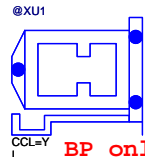
Screw hole should be D=4.03mm

MCP - VID,GFX-VID,CTRL, MSIC

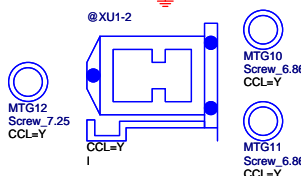
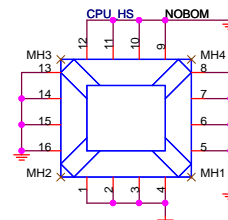
MCP-VID,CTRL,MSIC



LGA115X_CPU_COVER



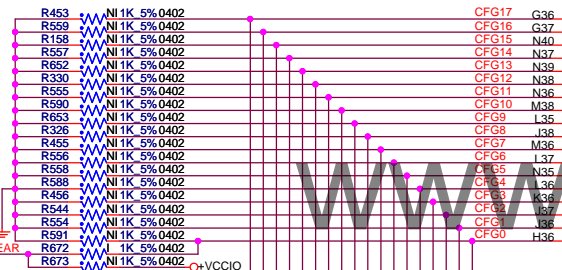
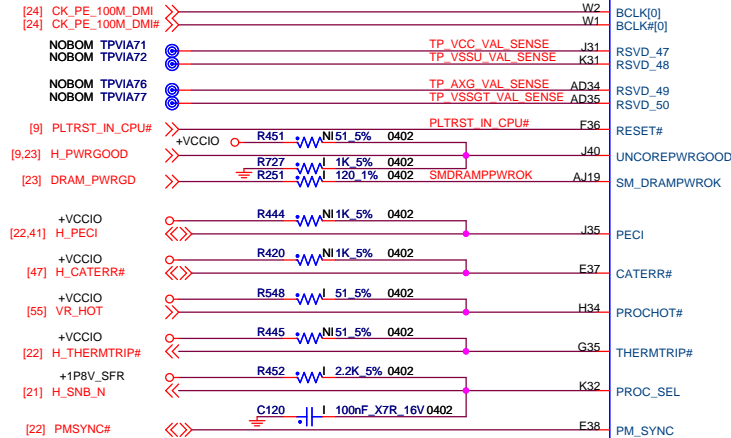
BP only



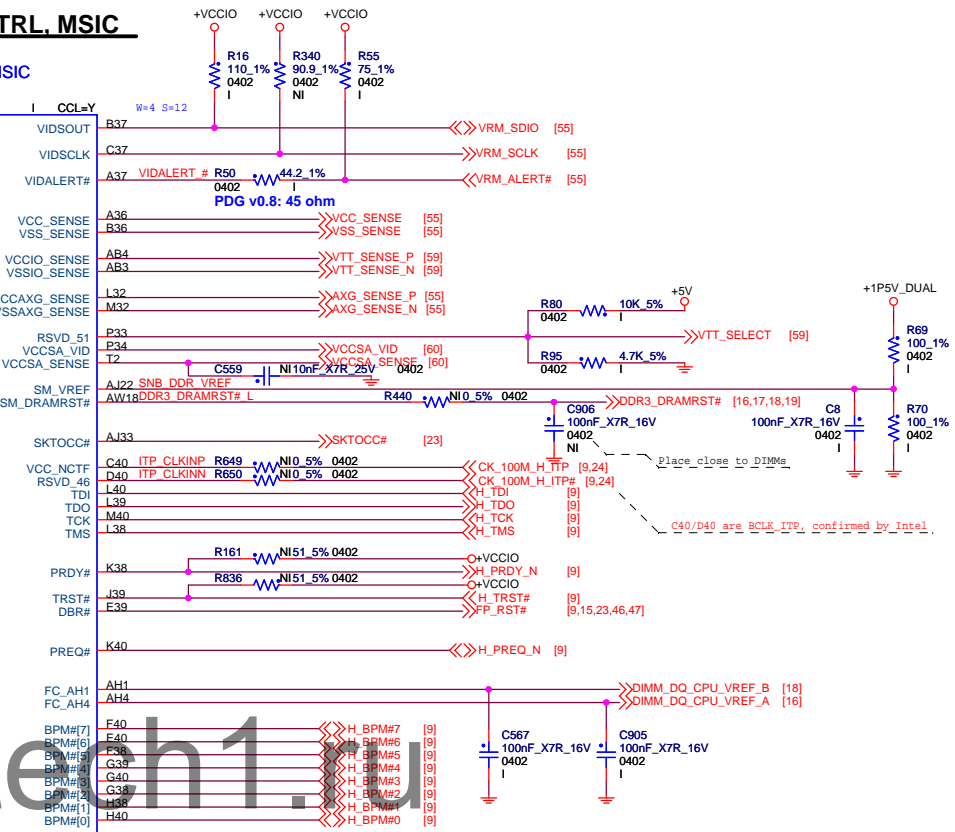
ILM & SCREWS

[9] XDP_EAR

[9] CFG0..17



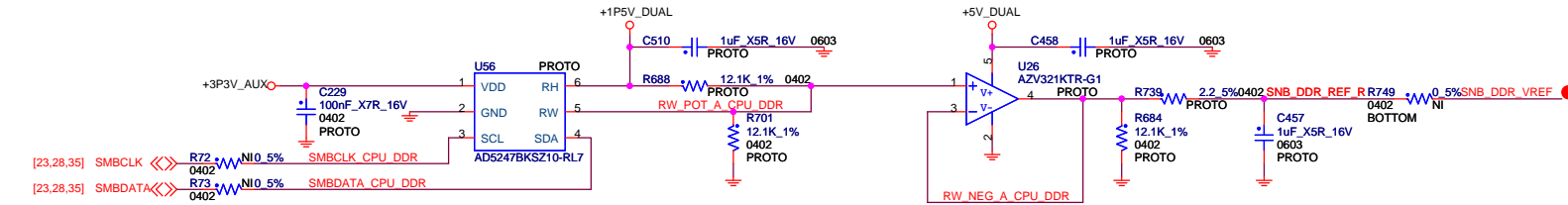
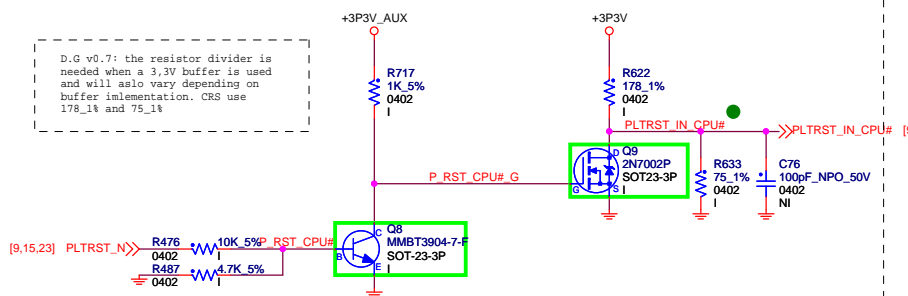
Socket_LGA_1155_15u_Black



CPU REST CIRCUITRY

DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC 1SF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS 1SF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

D.G v0.7: the resistor divider is needed when a 3.3V buffer is used and will also vary depending on buffer implementation. CRS use 178_1k and 75_1k



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Title: **MCP-CLK, CTRL, MISC, DEBUG**

Size: Document Number: Rev: **0.1**

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MCP - DDR3 CH-A

MCP - DDR3 CH-B

MCP-DDR3

[18,19] M_DB[0..63] <<<> M_DB[0..63]

MCP-DDR3

[16,17] M_DA[0..63] <<<> M_DA[0..63]

XU1A			CCL=Y		
M DA63	AE40	SA_DQ[63]	SA_MA[15]	AT20	M MAA A15
M DA62	AE39	SA_DQ[62]	SA_MA[14]	AU20	M MAA A14
M DA61	AG38	SA_DQ[61]	SA_MA[13]	AW32	M MAA A13
M DA60	AG39	SA_DQ[60]	SA_MA[12]	AT21	M MAA A12
M DA59	AE37	SA_DQ[59]	SA_MA[11]	AU21	M MAA A11
M DA58	AE38	SA_DQ[58]	SA_MA[10]	AV28	M MAA A10
M DA57	AG37	SA_DQ[57]	SA_MA[9]	AT22	M MAA A9
M DA56	AG40	SA_DQ[56]	SA_MA[8]	AV22	M MAA A8
M DA55	AJ40	SA_DQ[55]	SA_MA[7]	AU22	M MAA A7
M DA54	AJ39	SA_DQ[54]	SA_MA[6]	AT23	M MAA A6
M DA53	AL38	SA_DQ[53]	SA_MA[5]	AT24	M MAA A5
M DA52	AL39	SA_DQ[52]	SA_MA[4]	AV23	M MAA A4
M DA51	AJ37	SA_DQ[51]	SA_MA[3]	AW23	M MAA A3
M DA50	AJ38	SA_DQ[50]	SA_MA[2]	AW24	M MAA A2
M DA49	AL37	SA_DQ[49]	SA_MA[1]	AY24	M MAA A1
M DA48	AL40	SA_DQ[48]	SA_MA[0]	AV27	M MAA A0
M DA47	AN40	SA_DQ[47]			
M DA46	AN39	SA_DQ[46]			
M DA45	AR38	SA_DQ[45]			
M DA44	AR39	SA_DQ[44]			
M DA43	AN37	SA_DQ[43]			
M DA42	AN38	SA_DQ[42]			
M DA41	AR37	SA_DQ[41]			
M DA40	AR40	SA_DQ[40]			
M DA39	AJ37	SA_DQ[39]			
M DA38	AJ38	SA_DQ[38]			
M DA37	AY36	SA_DQ[37]			
M DA36	AW35	SA_DQ[36]			
M DA35	AJ36	SA_DQ[35]			
M DA34	AJ39	SA_DQ[34]			
M DA33	AW37	SA_DQ[33]			
M DA32	AJ35	SA_DQ[32]			
M DA31	AY39	SA_DQ[31]			
M DA30	AW39	SA_DQ[30]			
M DA29	AW37	SA_DQ[29]			
M DA28	AV37	SA_DQ[28]			
M DA27	AU39	SA_DQ[27]			
M DA26	AV39	SA_DQ[26]			
M DA25	AU37	SA_DQ[25]			
M DA24	AY37	SA_DQ[24]			
M DA23	AY38	SA_DQ[23]			
M DA22	AU35	SA_DQ[22]			
M DA21	AU38	SA_DQ[21]			
M DA20	AU32	SA_DQ[20]			
M DA19	AW35	SA_DQ[19]			
M DA18	AV35	SA_DQ[18]			
M DA17	AW33	SA_DQ[17]			
M DA16	AV32	SA_DQ[16]			
M DA15	AR11	SA_DQ[15]			
M DA14	AR12	SA_DQ[14]			
M DA13	AN33	SA_DQ[13]			
M DA12	AN32	SA_DQ[12]			
M DA11	AR4	SA_DQ[11]			
M DA10	AR3	SA_DQ[10]			
M DA9	AN1	SA_DQ[9]			
M DA8	AN1	SA_DQ[8]			
M DA7	AL3	SA_DQ[7]			
M DA6	AL2	SA_DQ[6]			
M DA5	AJ11	SA_DQ[5]			
M DA4	AJ12	SA_DQ[4]			
M DA3	AL4	SA_DQ[3]			
M DA2	AL3	SA_DQ[2]			
M DA1	AJ4	SA_DQ[1]			
M DA0	AJ3	SA_DQ[0]			

XU1B			CCL=Y		
M DB63	AF35	SB_DQ[63]	SB_MA[15]	AV16	M MAA B15
M DB62	AF33	SB_DQ[62]	SB_MA[14]	AY16	M MAA B14
M DB61	AJ34	SB_DQ[61]	SB_MA[13]	AR26	M MAA B13
M DB60	AJ35	SB_DQ[60]	SB_MA[12]	AT18	M MAA B12
M DB59	AE35	SB_DQ[59]	SB_MA[11]	AU17	M MAA B11
M DB58	AE34	SB_DQ[58]	SB_MA[10]	AN23	M MAA B10
M DB57	AH34	SB_DQ[57]	SB_MA[9]	AY17	M MAA B9
M DB56	AH35	SB_DQ[56]	SB_MA[8]	AL18	M MAA B8
M DB55	AM35	SB_DQ[55]	SB_MA[7]	AM18	M MAA B7
M DB54	AL31	SB_DQ[54]	SB_MA[6]	AP18	M MAA B6
M DB53	AM31	SB_DQ[53]	SB_MA[5]	AP19	M MAA B5
M DB52	AM32	SB_DQ[52]	SB_MA[4]	AK18	M MAA B4
M DB51	AL32	SB_DQ[51]	SB_MA[3]	AM19	M MAA B3
M DB50	AL35	SB_DQ[50]	SB_MA[2]	AM20	M MAA B2
M DB49	AR34	SB_DQ[49]	SB_MA[1]	AK24	M MAA B1
M DB48	AR35	SB_DQ[48]	SB_MA[0]		
M DB47	AR36	SB_DQ[47]			
M DB46	AR37	SB_DQ[46]			
M DB45	AR31	SB_DQ[45]			
M DB44	AR32	SB_DQ[44]			
M DB43	AP34	SB_DQ[43]			
M DB42	AP35	SB_DQ[42]			
M DB41	AP31	SB_DQ[41]			
M DB40	AP32	SB_DQ[40]			
M DB39	AM29	SB_DQ[39]			
M DB38	AM28	SB_DQ[38]			
M DB37	AP29	SB_DQ[37]			
M DB36	AP28	SB_DQ[36]			
M DB35	AL29	SB_DQ[35]			
M DB34	AL28	SB_DQ[34]			
M DB33	AR29	SB_DQ[33]			
M DB32	AR28	SB_DQ[32]			
M DB31	AP12	SB_DQ[31]			
M DB30	AR12	SB_DQ[30]			
M DB29	AL13	SB_DQ[29]			
M DB28	AL12	SB_DQ[28]			
M DB27	AP13	SB_DQ[27]			
M DB26	AR13	SB_DQ[26]			
M DB25	AM13	SB_DQ[25]			
M DB24	AM12	SB_DQ[24]			
M DB23	AR9	SB_DQ[23]			
M DB22	AP9	SB_DQ[22]			
M DB21	AR6	SB_DQ[21]			
M DB20	AP6	SB_DQ[20]			
M DB19	AR10	SB_DQ[19]			
M DB18	AP10	SB_DQ[18]			
M DB17	AR7	SB_DQ[17]			
M DB16	AR7	SB_DQ[16]			
M DB15	AL9	SB_DQ[15]			
M DB14	AL9	SB_DQ[14]			
M DB13	AM6	SB_DQ[13]			
M DB12	AL6	SB_DQ[12]			
M DB11	AM10	SB_DQ[11]			
M DB10	AM7	SB_DQ[10]			
M DB9	AL7	SB_DQ[9]			
M DB8	AJ7	SB_DQ[8]			
M DB7	AJ7	SB_DQ[7]			
M DB6	AJ6	SB_DQ[6]			
M DB5	AG6	SB_DQ[5]			
M DB4	AG5	SB_DQ[4]			
M DB3	AJ8	SB_DQ[3]			
M DB2	AJ9	SB_DQ[2]			
M DB1	AG8	SB_DQ[1]			
M DB0	AG7	SB_DQ[0]			

Add the corresponding CM&CTRL&CLK signals for the Channel A DIMM1

Add the corresponding CM&CTRL&CLK signals for the Channel B DIMM1

Socket_LGA 1155_15u_Black

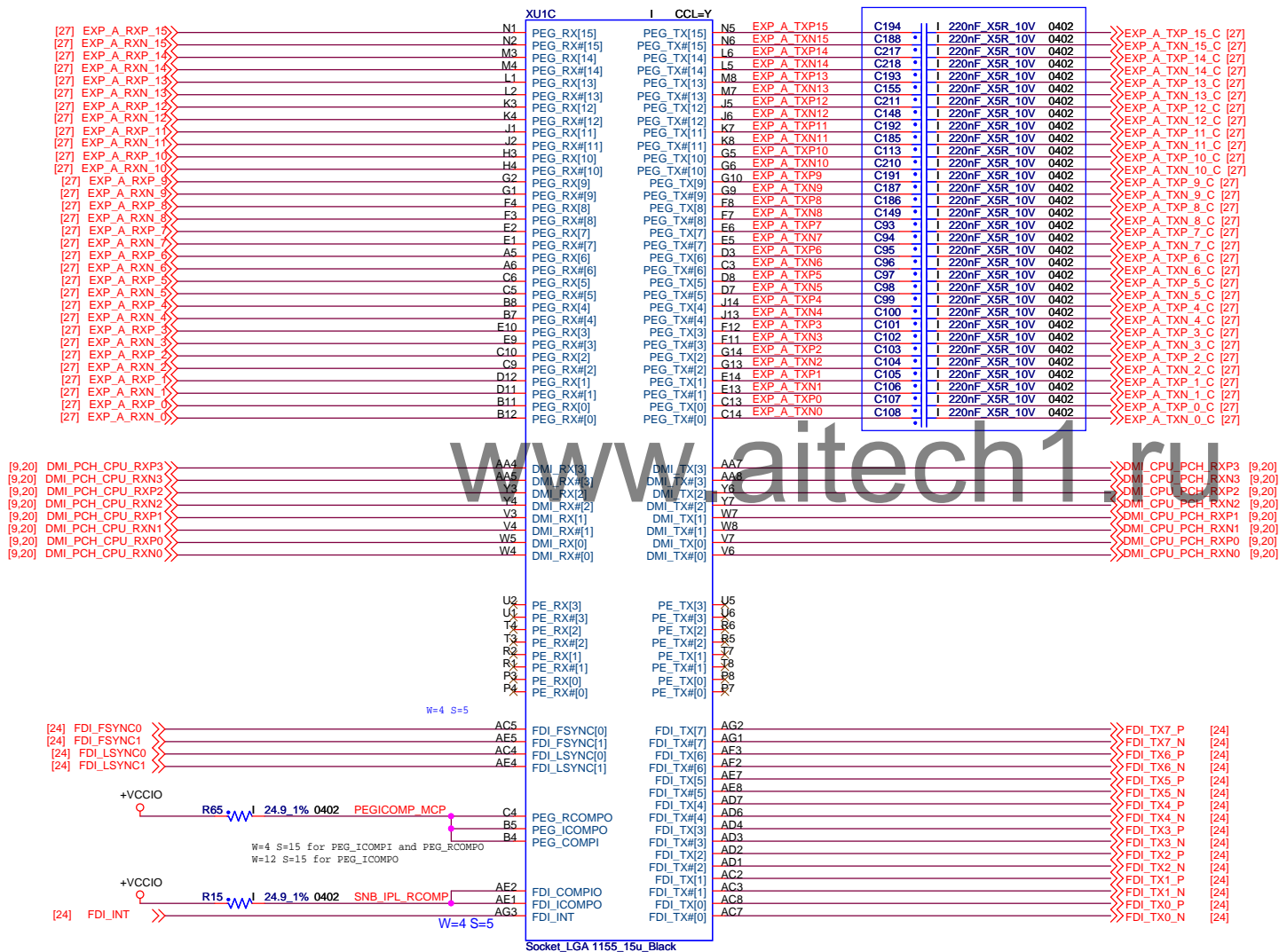
Socket_LGA 1155_15u_Black

Routing bundles are differential pairs that share a common equalization register. Differential pair 0 and 1 are a bundle, differential pair 2 and 3 are a bundle, and so on. For example on PCIE: PEG_TX_#/#[0] and PEG_TX_#/#[1] or PEG_TX_#/#[2] and PEG_TX_#/#[3] are two examples. Length match pairs in a bundle to within 0.4 inch.

MCP - PCIE,DMI,FDI

MCP-PEG,PE,DMI,FDI

Close to Slot



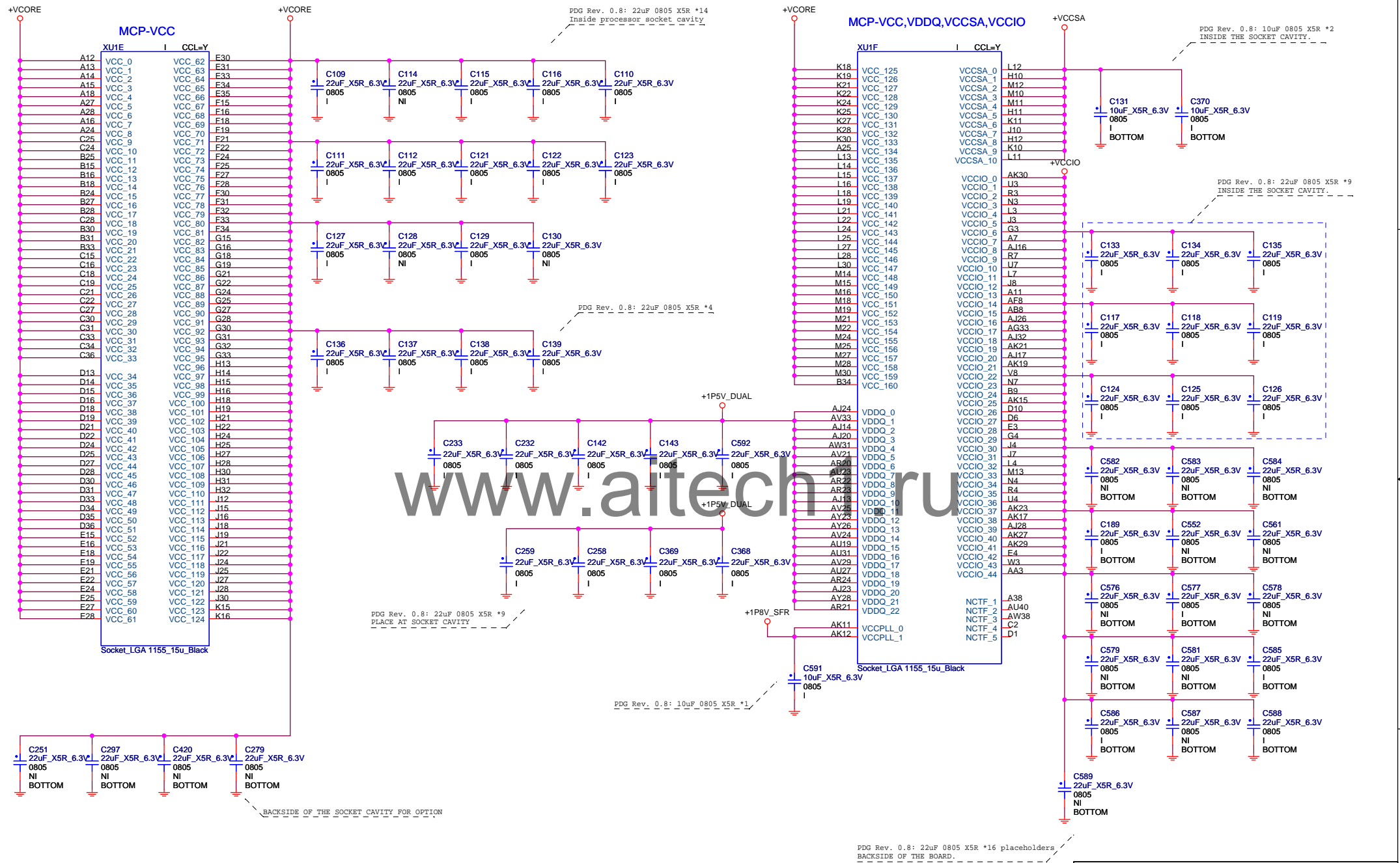
SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R65.
ROUTE B5 TO R65 AS A SEPERATE 12 MIL TRACE

FOXCONN
Hon Hai Precision Industry Co. Ltd.
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Title
MCP- PCIE, DMI, FDI

Size
Custom
Document Number
Magellan-H67
Rev
0.1

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+VCC_AXG

MCP-VCCAXG,RSVD

XU1G

I CCL=Y

AC33	VCCAXG_0	RSVD_0	H7
AC34	VCCAXG_1	RSVD_1	K9
AC35	VCCAXG_2	RSVD_2	H8
AC36	VCCAXG_3	RSVD_3	AF4
AC37	VCCAXG_4	RSVD_4	AE6
AC38	VCCAXG_5	RSVD_5	T11
AC39	VCCAXG_6	RSVD_6	B33
AC40	VCCAXG_7	RSVD_7	B34
Y33	VCCAXG_8	RSVD_8	L31
Y34	VCCAXG_9	RSVD_9	L34
Y35	VCCAXG_10	RSVD_10	M34
Y36	VCCAXG_11	RSVD_11	N33
Y37	VCCAXG_12	RSVD_12	AW2
Y38	VCCAXG_13	RSVD_13	B35
Y39	VCCAXG_14	RSVD_14	B37
Y40	VCCAXG_15	RSVD_15	B39
Y41	VCCAXG_16	RSVD_16	B34
Y42	VCCAXG_17	RSVD_17	B36
Y43	VCCAXG_18	RSVD_18	B38
Y44	VCCAXG_19	RSVD_19	B40
Y45	VCCAXG_20	RSVD_20	C39
Y46	VCCAXG_21	RSVD_21	D38
Y47	VCCAXG_22	RSVD_22	AT14
Y48	VCCAXG_23	RSVD_23	AY3
Y49	VCCAXG_24	RSVD_24	B39
Y50	VCCAXG_25	RSVD_25	AD37
Y51	VCCAXG_26	RSVD_26	AJ31
Y52	VCCAXG_27	RSVD_27	AJ29
Y53	VCCAXG_28	RSVD_28	AB7
Y54	VCCAXG_29	RSVD_29	AN20
Y55	VCCAXG_30	RSVD_30	AJ30
Y56	VCCAXG_31	RSVD_31	N34
Y57	VCCAXG_32	RSVD_32	AY10
Y58	VCCAXG_33	RSVD_33	AP20
Y59	VCCAXG_34	RSVD_34	C38
Y60	VCCAXG_35	RSVD_35	B34
Y61	VCCAXG_36	RSVD_36	AV34
Y62	VCCAXG_37	RSVD_37	AW34
Y63	VCCAXG_38	RSVD_38	AJ11
Y64	VCCAXG_39	RSVD_39	AJ10
Y65	VCCAXG_40	RSVD_40	AB6
Y66	VCCAXG_41	RSVD_41	AT11
Y67	VCCAXG_42	RSVD_42	B
Y68	VCCAXG_43	RSVD_43	L34
Y69	VCCAXG_44	RSVD_44	L9
Y70	VCCAXG_45	RSVD_45	X

Socket_LGA 1155_15u_Black

MCP-VSS

XU1H

CCL=Y

C17	VSS_0	VSS_93	AN6
C20	VSS_1	VSS_94	AJ5
D37	VSS_2	VSS_95	J11
D4	VSS_3	VSS_96	G11
D5	VSS_4	VSS_97	C12
K13	VSS_5	VSS_98	E11
K2	VSS_6	VSS_99	E12
AF36	VSS_7	VSS_100	Y8
T11	VSS_8	VSS_101	AA6
P1	VSS_9	VSS_102	AF34
M1	VSS_10	VSS_103	AA36
K1	VSS_11	VSS_104	AA36
H1	VSS_12	VSS_105	AA36
F1	VSS_13	VSS_106	AA36
D2	VSS_14	VSS_107	AA36
B6	VSS_15	VSS_108	AA36
C8	VSS_16	VSS_109	AA36
D9	VSS_17	VSS_110	AA36
F10	VSS_18	VSS_111	AA36
Y5	VSS_19	VSS_112	AA36
R8	VSS_20	VSS_113	AA36
U8	VSS_21	VSS_114	AA36
N8	VSS_22	VSS_115	AA36
G7	VSS_23	VSS_116	AA36
F5	VSS_24	VSS_117	AA36
E7	VSS_25	VSS_118	AA36
C7	VSS_26	VSS_119	AA36
B10	VSS_27	VSS_120	AA36
E36	VSS_28	VSS_121	AA36
F13	VSS_29	VSS_122	AA36
G34	VSS_30	VSS_123	AA36
K37	VSS_31	VSS_124	AA36
K5	VSS_32	VSS_125	AA36
K6	VSS_33	VSS_126	AA36
F2	VSS_34	VSS_127	AA36
F20	VSS_35	VSS_128	AA36
F23	VSS_36	VSS_129	AA36
F26	VSS_37	VSS_130	AA36
F29	VSS_38	VSS_131	AA36
F35	VSS_39	VSS_132	AA36
H2	VSS_40	VSS_133	AA36
H33	VSS_41	VSS_134	AA36
H39	VSS_42	VSS_135	AA36
H5	VSS_43	VSS_136	AA36
H6	VSS_44	VSS_137	AA36
J17	VSS_45	VSS_138	AA36
AL36	VSS_46	VSS_139	AA36
AN35	VSS_47	VSS_140	AA36
AJ36	VSS_48	VSS_141	AA36
AP37	VSS_49	VSS_142	AA36
AP36	VSS_50	VSS_143	AA36
AN33	VSS_51	VSS_144	AA36
AT31	VSS_52	VSS_145	AA36
AT35	VSS_53	VSS_146	AA36
AT32	VSS_54	VSS_147	AA36
AP22	VSS_55	VSS_148	AA36
AT6	VSS_56	VSS_149	AA36
AT7	VSS_57	VSS_150	AA36
AM4	VSS_58	VSS_151	AA36
AL5	VSS_59	VSS_152	AA36
AM5	VSS_60	VSS_153	AA36
AK7	VSS_61	VSS_154	AA36
AK6	VSS_62	VSS_155	AA36
AH5	VSS_63	VSS_156	AA36
AF5	VSS_64	VSS_157	AA36
AC6	VSS_65	VSS_158	AA36
AH8	VSS_66	VSS_159	AA36
AK35	VSS_67	VSS_160	AA36
AN32	VSS_68	VSS_161	AA36
AN24	VSS_69	VSS_162	AA36
AL6	VSS_70	VSS_163	AA36
AN14	VSS_71	VSS_164	AA36
AN11	VSS_72	VSS_165	AA36
AP14	VSS_73	VSS_166	AA36
AT13	VSS_74	VSS_167	AA36
AV11	VSS_75	VSS_168	AA36
AW16	VSS_76	VSS_169	AA36
AT17	VSS_77	VSS_170	AA36
AV17	VSS_78	VSS_171	AA36
AY18	VSS_79	VSS_172	AA36
AU26	VSS_80	VSS_173	AA36
AR19	VSS_81	VSS_174	AA36
AR18	VSS_82	VSS_175	AA36
AN17	VSS_83	VSS_176	AA36
AT15	VSS_84	VSS_177	AA36
AR17	VSS_85	VSS_178	AA36
AR14	VSS_86	VSS_179	AA36
AR36	VSS_87		
AT25	VSS_88		
AP5	VSS_89		
AM36	VSS_90	VSS_NCTF_1	B3
AT37	VSS_91	VSS_NCTF_2	A4
AN7	VSS_92	VSS_NCTF_3	AV39
		VSS_NCTF_4	AY37

Socket_LGA 1155_15u_Black

MCP-VSS

XU1I

CCL=Y

AG36	VSS_180	VSS_270	R39
A29	VSS_181	VSS_271	J20
A23	VSS_182	VSS_272	J23
A26	VSS_183	VSS_273	J26
A35	VSS_184	VSS_274	J29
B29	VSS_185	VSS_275	J32
AT34	VSS_186	VSS_276	AJ18
Y8	VSS_187	VSS_277	AT4
AA33	VSS_188	VSS_278	AP4
AA34	VSS_189	VSS_279	AP1
AA35	VSS_190	VSS_280	AM2
AA36	VSS_191	VSS_281	AC1
AA36	VSS_192	VSS_282	AK1
AA36	VSS_193	VSS_283	AT27
AA36	VSS_194	VSS_284	AN31
AA36	VSS_195	VSS_285	C23
AA36	VSS_196	VSS_286	AN34
AA36	VSS_197	VSS_287	AN36
AA36	VSS_198	VSS_288	AN5
AA36	VSS_199	VSS_289	AN8
AA36	VSS_200	VSS_290	AL19
AA36	VSS_201	VSS_291	AH40
AA36	VSS_202	VSS_292	AU15
AA36	VSS_203	VSS_293	AP27
AA36	VSS_204	VSS_294	AK28
AA36	VSS_205	VSS_295	AT2
AA36	VSS_206	VSS_296	AH2
AA36	VSS_207	VSS_297	AT30
AA36	VSS_208	VSS_298	AT33
AA36	VSS_209	VSS_299	AT36
AA36	VSS_210	VSS_300	AT38
AA36	VSS_211	VSS_301	AT5
AA36	VSS_212	VSS_302	AP17
AA36	VSS_213	VSS_303	AV3
AA36	VSS_214	VSS_304	AE1
AA36	VSS_215	VSS_305	B23
AA36	VSS_216	VSS_306	AY4
AA36	VSS_217	VSS_307	C26
AA36	VSS_218	VSS_308	C29
AA36	VSS_219	VSS_309	C32
AA36	VSS_220	VSS_310	C35
AA36	VSS_221	VSS_311	AD5
AA36	VSS_222	VSS_312	AD8
AA36	VSS_223	VSS_313	AE3
AA36	VSS_224	VSS_314	AF40
AA36	VSS_225	VSS_315	AE6
AA36	VSS_226	VSS_316	AM27
AA36	VSS_227	VSS_317	B38
AA36	VSS_228	VSS_318	AH33
AA36	VSS_229	VSS_319	AH38
AA36	VSS_230	VSS_320	AT12
AA36	VSS_231	VSS_321	AY35
AA36	VSS_232	VSS_322	AN27
AA36	VSS_233	VSS_323	AT29
AA36	VSS_234	VSS_324	AK5
AA36	VSS_235	VSS_325	AK8
AA36	VSS_236	VSS_326	AL11
AA36	VSS_237	VSS_327	AJ8
AA36	VSS_238	VSS_328	AV6
AA36	VSS_239	VSS_329	AL24
AA36	VSS_240	VSS_330	AM23
AA36	VSS_241	VSS_331	AM40
AA36	VSS_242	VSS_332	AN10
AA36	VSS_243	VSS_333	AK4
AA36	VSS_244	VSS_334	AP40
AA36	VSS_245	VSS_335	AT40
AA36	VSS_246	VSS_336	AT39
AA36	VSS_247	VSS_337	AJ34
AA36	VSS_248	VSS_338	AP11
AA36	VSS_249	VSS_339	AV38
AA36	VSS_250	VSS_340	AR5
AA36	VSS_251	VSS_341	AJ4
AA36	VSS_252	VSS_342	AR27
AA36	VSS_253	VSS_343	AP25
AA36	VSS_254	VSS_344	AN9
AA36	VSS_255	VSS_345	AT28
AA36	VSS_256	VSS_346	AM3
AA36	VSS_257	VSS_347	AY8
AA36	VSS_258	VSS_348	AT3
AA36	VSS_259	VSS_349	AP30
AA36	VSS_260	VSS_350	AT1
AA36	VSS_261	VSS_351	AW6
AA36	VSS_262	VSS_352	AT8
AA36	VSS_263	VSS_353	AM11
AA36	VSS_264	VSS_354	AK36
AA36	VSS_265	VSS_355	AR11
AA36	VSS_266	VSS_356	AH3
AA36	VSS_267	VSS_357	AK10
AA36	VSS_268	VSS_358	AK9
AA36	VSS_269	VSS_359	AM1

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Intel PCH Debugging Connector

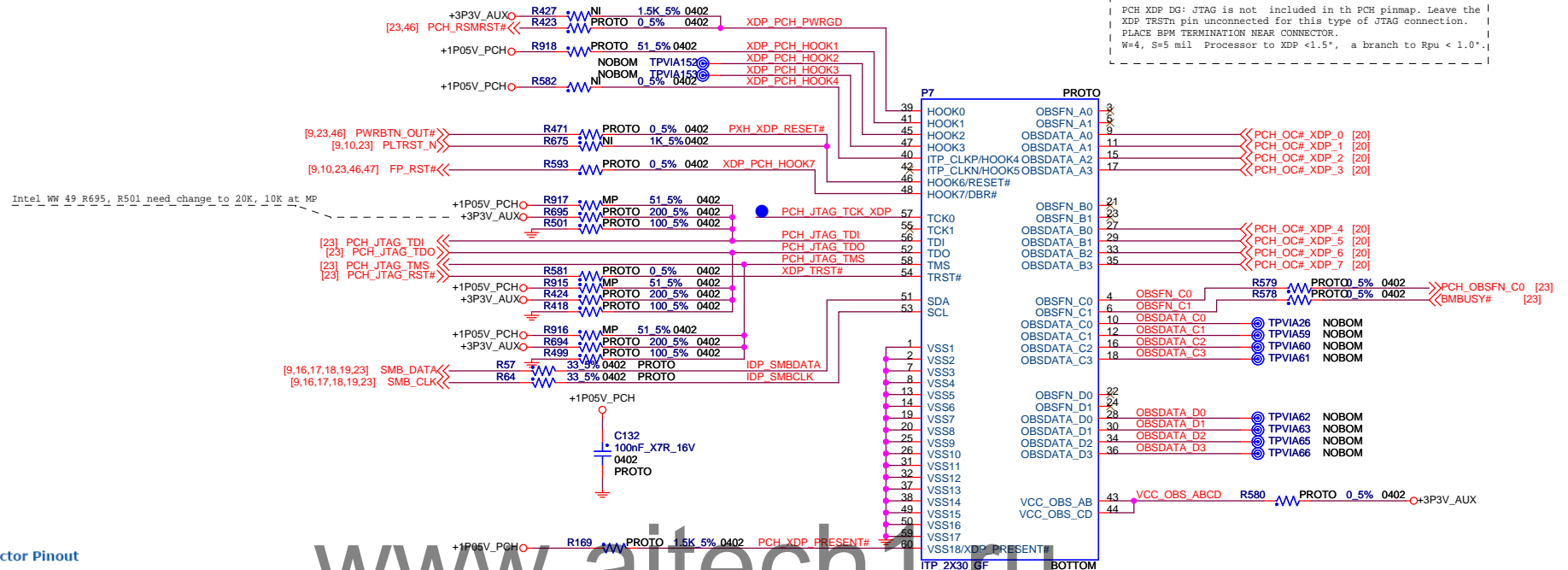
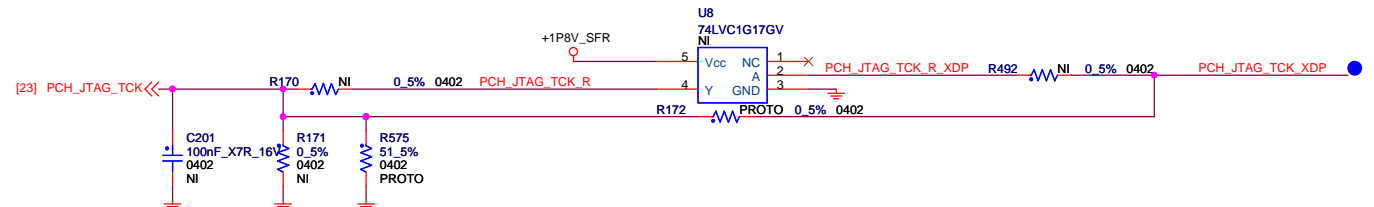


Table 4-1. PCH XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		4	GND	GND	NA	
3	OBSFN_A0	Open	NA		2	OBSFN_C0	GPI015	1	PCH
5	OBSFN_A1	Open	NA		6	OBSFN_C1	BMBUSY# / GPI00	1	PCH
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0	OC0# / GPIO59	1	PCH	10	OBSDATA_C0	MGP107 / GPIO28	1	PCH
11	OBSDATA_A1	OC1# / GPIO40	1	PCH	12	OBSDATA_C1	GPI035	1	PCH
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	OC2# / GPIO41	1	PCH	16	OBSDATA_C2	SATA0GP / GPIO21	1	PCH
17	OBSDATA_A3	OC3# / GPIO42	1	PCH	18	OBSDATA_C3	SATA1GP / GPIO19	1	PCH
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0	Open	NA		22	OBSFN_D0	Open	NA	
23	OBSFN_B1	Open	NA		24	OBSFN_D1	Open	NA	
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	OC4# / GPIO43	1	PCH	28	OBSDATA_D0	SATA2GP / GPIO16	1	PCH
29	OBSDATA_B1	OC5# / GPIO9	1	PCH	30	OBSDATA_D1	SATA3GP / GPIO37	1	PCH
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	OC6# / GPIO10	1	PCH	34	OBSDATA_D2	SATA4GP / GPIO16	1	PCH
35	OBSDATA_B3	OC7# / GPIO14	1	PCH	36	OBSDATA_D3	SATA5GP / GPIO49	1	PCH
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	RSMRST#	1	PCH	40	ITPCLK/HOOK4	Open	NA	
41	HOOK1	BS_FWRGO_RST#	0	system	42	ITPCLK# / HOOK5	Open	NA	
43	VCC_OBS_AB	VccSus3_3	NA		44	VCC_OBS_CD	VccSus3_3	NA	
45	HOOK2	Open	1		46	HOOK6 / RESET#	RSMRST#	1	PCH
47	HOOK3	Open	NA		48	HOOK7/DBR#	SYS_RESET#	0	PCH
49	GND	GND	NA		50	GND	GND	NA	
51	SDA	SDA	I/O	system	52	TDO	JTAG_TDO	1	PCH
53	SCL	SCL	I/O	system	54	TRSTn	Open	NA	
55	TCR1	Open	NA		56	TDI	JTAG_TDI	0	PCH
57	TCR0	JTAG_TCK	0	PCH	58	TMS	JTAG_TMS	0	PCH
59	GND	GND	NA		60	GND	GND (or XDP_PRESN T# if required)	NA	

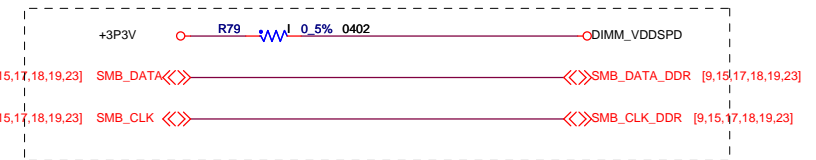


In Subject: Ibox peak JTAG requirements

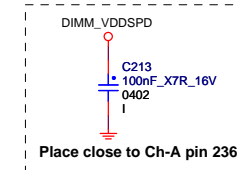
- In addition to the changes shown in the WW35 MOW Intel recommends customers implement the changes below on their platforms to support JTAG debug and boundary scan capabilities. These changes will be reflected in future CRB schematics and the Debug Port Design Guide.


- a) JTAG_TDI, JTAG_TDO, JTAG_TMS, TRST# require a strong pull-ups to a 1.05V.
- a) Pre-production and/or development systems should be connected to a 1.05 V sus rail, or Thevenin equivalent derived from 3.3 V sus. This connection will insure Intel supported debug is functional, however it will draw power in Sx states and thus is not recommended for production
- b) Production systems should include a 51 ohm pull-up to 1.05 Ore. In this configuration power draw in Sx states is minimized, and JTAG boundary Scan functional. However, Intel supported debug via this interface is. Production layouts should include sites for connection to a 1.05V sus rail, but components should not be stuffed.
- c) Intel recommends JTAG_TDO have a placeholder pull-up to 1.05V sus and core rails. The pull-up resistor pads should be left un-stuffed for ES1 due to an issue where JTAG_TDO will drive 3.3V signaling level instead of 1.05V.

Memory module install rule: furthest slot from CPU is the 1st, then closest slot.



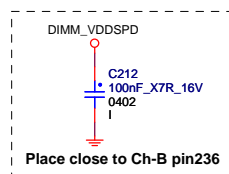
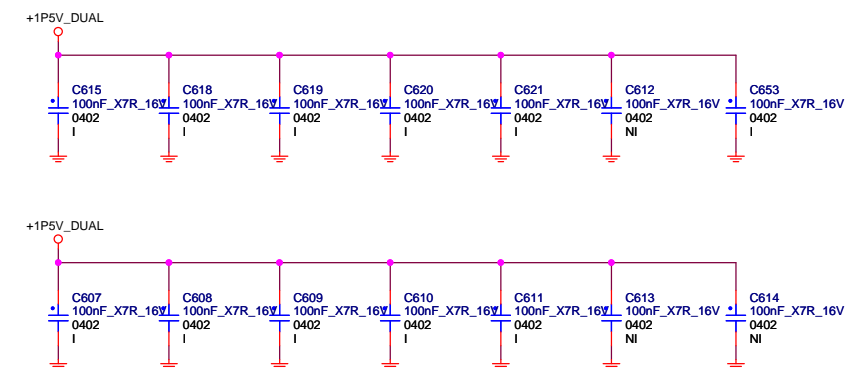
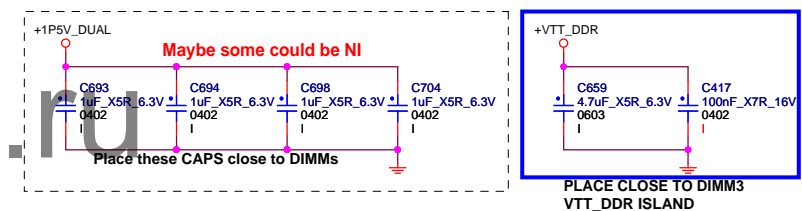
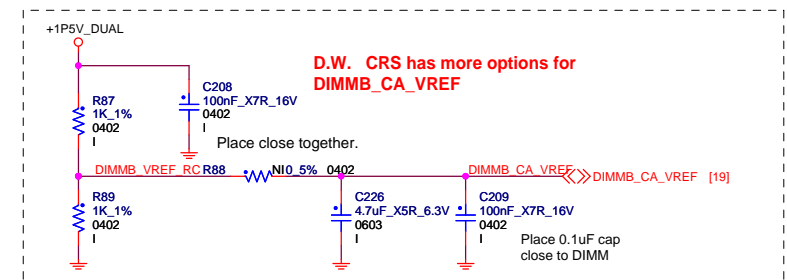
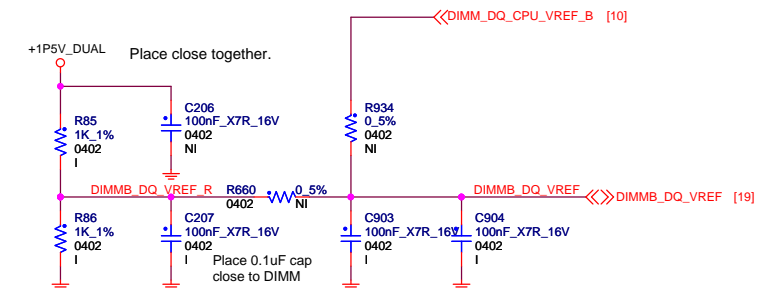
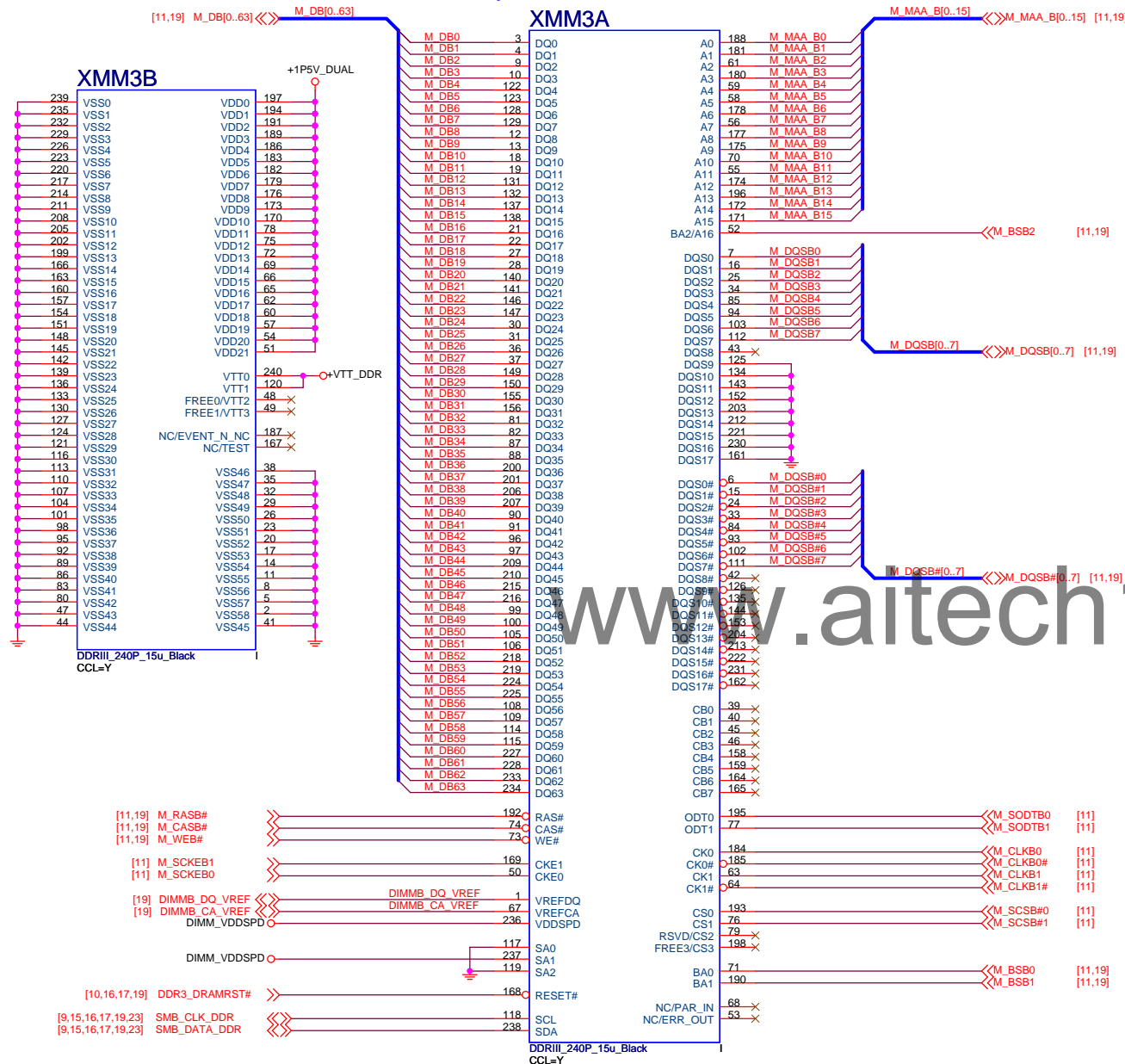
Memory module install rule: furthest slot from CPU is the 1st, then closest slot.



		Hon Hai Precision Industry Co. Ltd.	
Foxconn CMMSG Foxconn WuHan China		Phone: 755-28128988 Ext:22260 Fax: +86-755-2812-8988	
Title DDR3 CH-A DIMM2			
Size Custom	Document Number Magellan-H67		Rev 0.1
Page Modified: Tuesday, August 16, 2011 08:34:27 (UTC/GMT) Sheet 17 of 66			

DIMM Slot Sequence from MCP: CHA DIMM0 (XMM1), CHA DIMM1(XMM2), CHB DIMM0(XMM3), CHB DIMM1(XMM4).

Memory module install rule: furthest slot from CPU is the 1st, then closest slot.

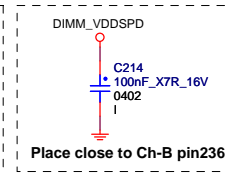
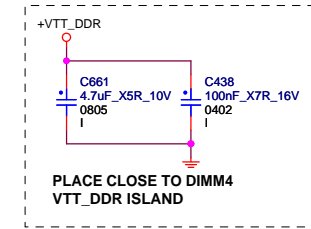
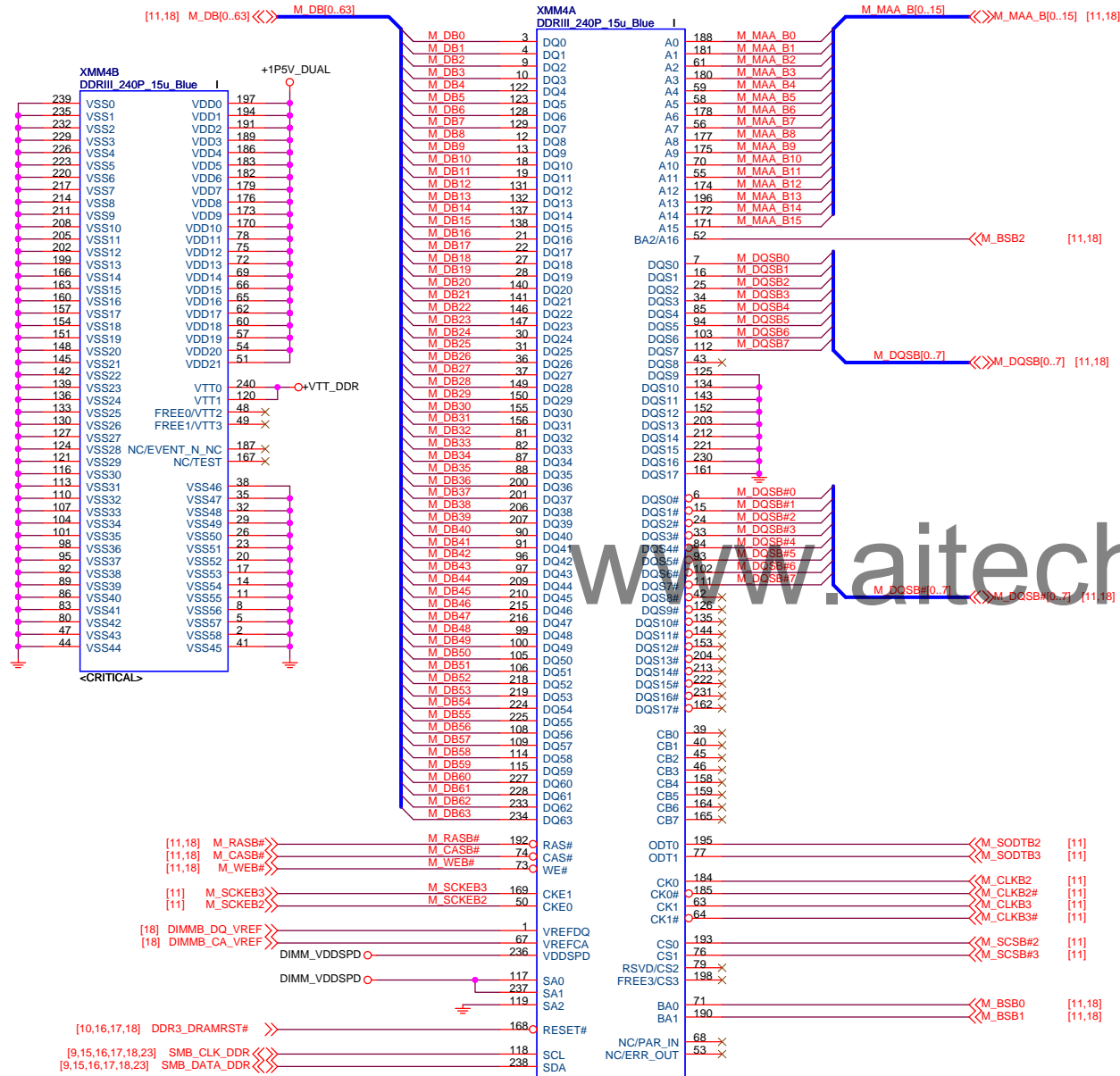


SPD ADDRESS: 010
SMBUS ADDRESS: A4

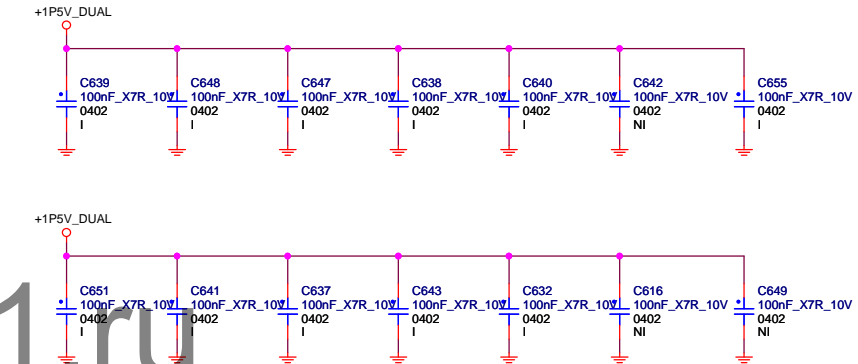
DDR3_CHB_DIMM1Socket Color: Blue 4rd DIMM slot from CPU

DIMM Slot Sequence from MCP: CHA DIMM0 (XMM1), CHA DIMM1(XMM2), CHB DIMM0(XMM3), CHB DIMM1(XMM4).

Memory module install rule: furthest slot from CPU is the 1st, then closest slot.

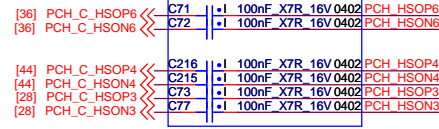


Place close to Ch-B pin236

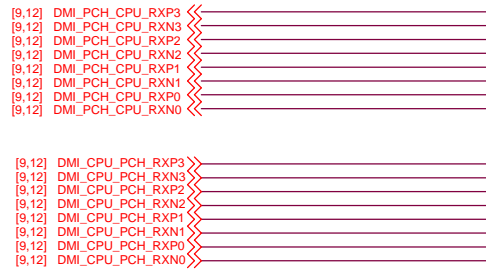


The probing point requires populating a resistor stuffing option that can be used to break the path to the device very near the device pins and ideally terminate each line (TX+/TX-) to ground through a 50 Ohms 1% resistor. Also, an AC coupling capacitor is required near the device pins. The resistor package/footprint must be as small as possible, preferably size 0402. The population of a 50-Ohm resistor, as shown in Figure 4-5,

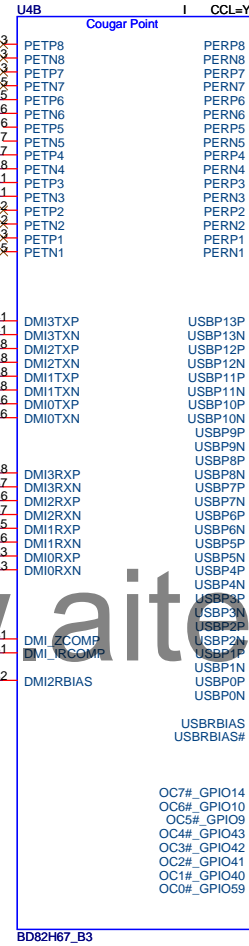
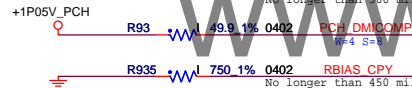
Close to Slot/Device



It is highly recommended to have DMI on surfaced vias (not buried).



PDG v0.8: The DMI compensation pins should be tied together and connected to the PCH 1.05-V rail (Vcc1_05_Filter) via a 49.9 ohm, 1% resistor (No longer than 500 mils).



PCIe port 7 & 8 are disable on H61

USB port 6 & 7, 12 & 13 are disable on H61

Add USB_13, USB_12 as rear USB ports

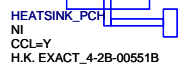
Add OC#7 as OC_protect port 12,13 of EHCI2

USB ports 6 and 7 are disabled on 12 port SKU's. (B65)

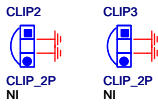
- EHCI1# Port 0-7
EHCI2# Port 8-13
- NOTES:
1. OC# pins are not 5 V tolerant.
 2. OC# pins must be shared between ports
 3. OC#[3:0] can only be used for EHCI Controller 1
 4. OC#[4:7] can only be used for EHCI Controller 2

EHCI#1: Device 29 Function 0; EHCI#2 Device 26 Function 0
Port 0-Port7: EHCI1 Port0 RMH1
Port 8-Port13: EHCI2 Port0 RMH2

4-2B-00551B



AVL:
VERICON_CX91A



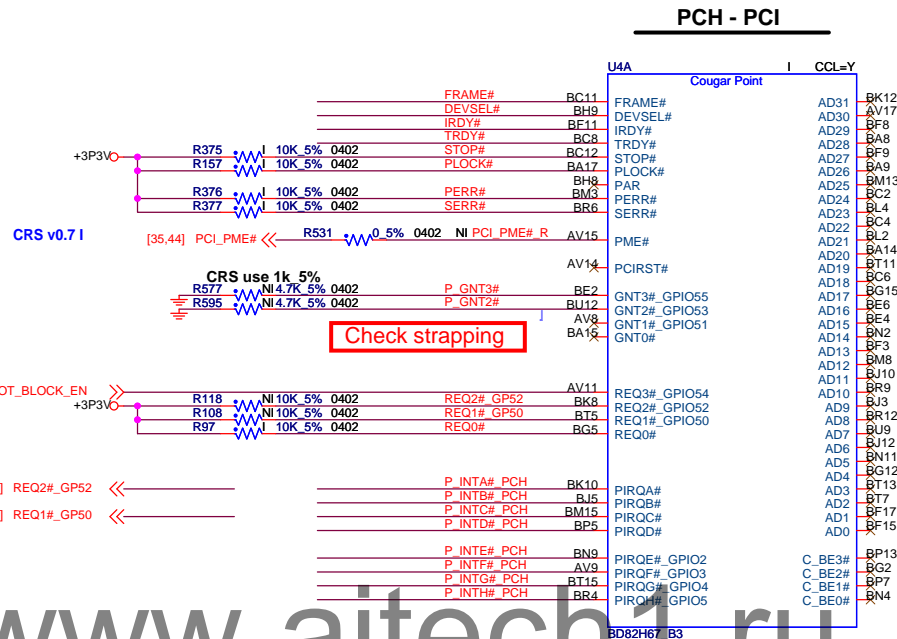
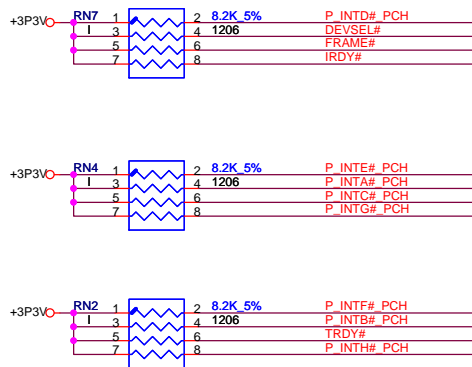
FOXCONN Hon Hai Precision Industry Co. Ltd.

Foxconn CMMSG
6F., No.32, Zhongcheng Rd., Tucheng City, Taipei County 23674, Taiwan, R.O.C. TEL: 886-2-8076-1055 FAX: 886-2-7075-7901

Title: **PCH- DMI, PCIe, USB**

Size: Document Number
Custord: **Magellan-H67**

Page Modified: Tuesday, August 16, 2011 08:34:26 (UTC/GMT) Sheet 20 of 66



GNT3:TOP-BLOCK SWAP OVERRIDE INTERNAL PULL UP 20K
A weak internal pull up, disabled after PLTRST# deasserts. A16 SWAP OVERRIDE:OVERRIDE IF SAMPLED LOW

GNT2: EST srp for server only. Do not pull low

BOOT DEVICE	GNT1#	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI (Default)	1	1

GNT1#: has a weak internal pull up,20k.
SATA1GP: has a weak internal pull up,TBD..

PDG V0.7 check list:

Default (SPI):

Left both SATA1GP/GPIO19 and GNT0# floating.No pull up required.

Boot from PCI:

Connect GNT0# to ground with 1k Ohm pulldownresistor.

Leave SATA1GP/GPIO19 Floating.

Boot from LPC:

Connect both SATA1GP/GPIO19 and GNT0# to ground with 1k Ohm pull-down resistor.

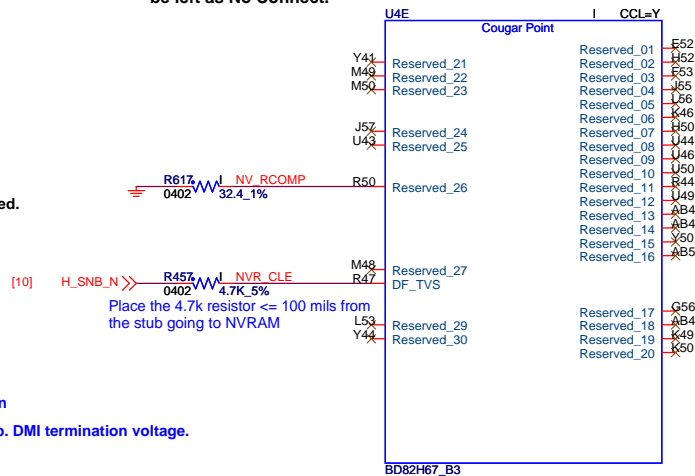
EDS v0.5 page 70: NV_CLE has a weak internal pull up

EDS v0.5 page 77: NV_CLE / NV_ALE has a 20 k internal pull down

PDG v0.7 check list page 379: NV_CLE has a weak internal pull up. DMI termination voltage.

For future processor compatibility, the PROC_SEL should be connected to the NV_CLE pin on the PCH through an isolation resistor of 4.7k ohm and a 2.2k ohm pull up to V_NAND_IO. Place the 4.7k resistor <= 100 mils from the stub going to NVRAM connector. Refer Figure 5-4 below for implementation

PDG:If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.



Non-Pull-up have serial 8.2K @OtherPage

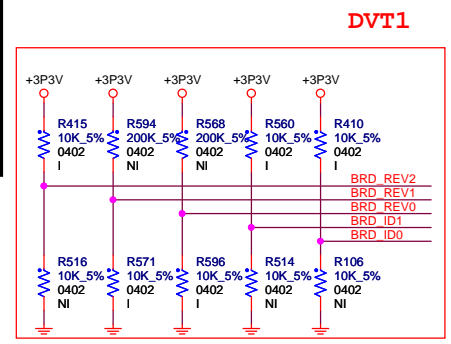
EVT1
[43] LPT_DET# >>

[43] COMM_B_DETECT# >>

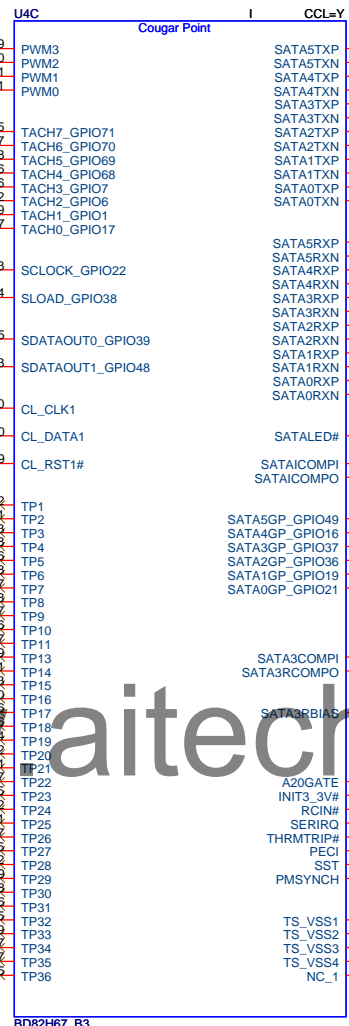
SLP_SUS# is a signal on PCH which indicate the system in deep sleep state. The deep sleep state is a lower power, limited wake features supported state where the Suspend well is powered off and only the DSW will in PCH remains powered.

BRD_REV[2:0]:	
000	EVT
001	EVT2
010	DVT1
011	DVT2
100	1.00 (PVT/MVB)
101	1.10 (ECN1)
110	1.20 (ECN2)
111	1.30 (ECN3)

BRD_ID[1:0]:	
00	NA
01	NA
10	NA
11	NA



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SATA port 2 & 3 are disable on H61

Full-high @ Audio Page.

SATACOMPO and the SATACOMPI pins be shorted at the package and then routed on the top layer to one end of a 37.4 ohm $\pm 1\%$ resistor to VccIO.

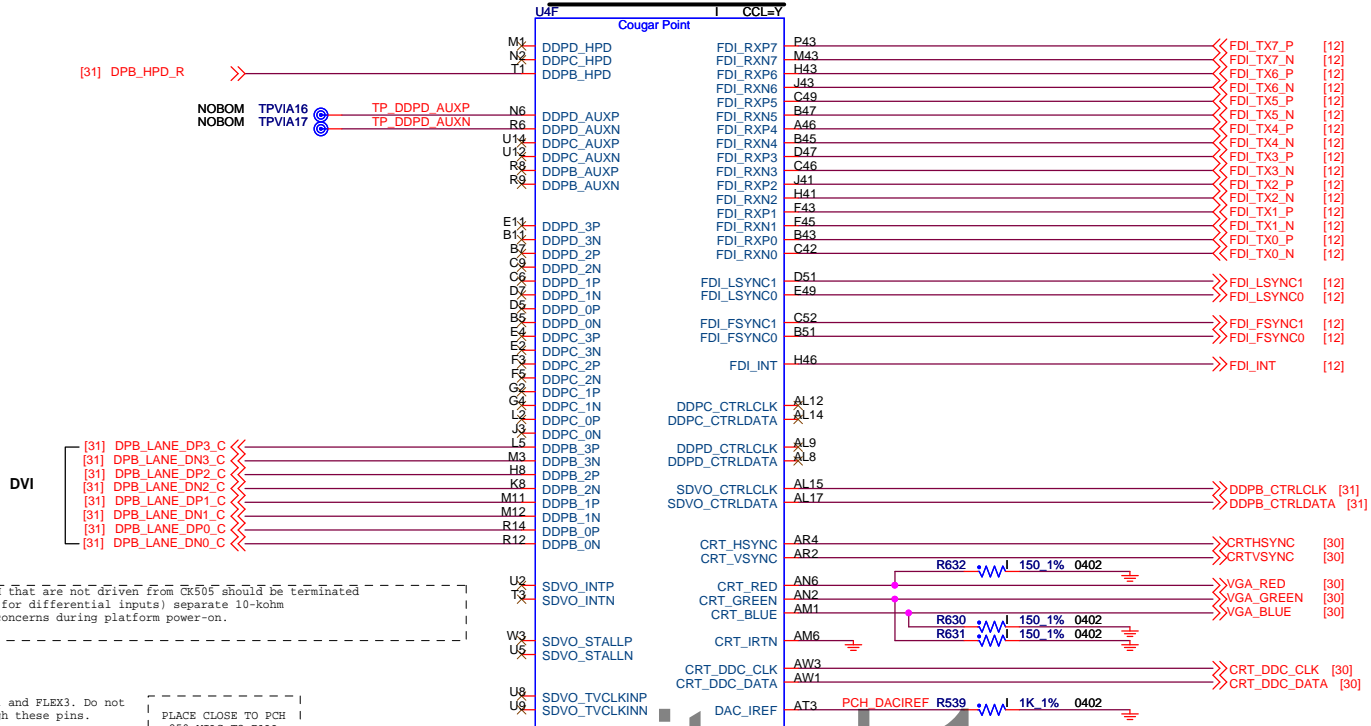
SATA3COMPO and the SATA3COMPI pins should be shorted at the package and then routed on the top layer to one end of a 49.9 ohm $\pm 1\%$ resistor to VccIO

CRS rev0.7 remark: CONNECT TO GND ON CRB PINS A54,A52,F57,D57

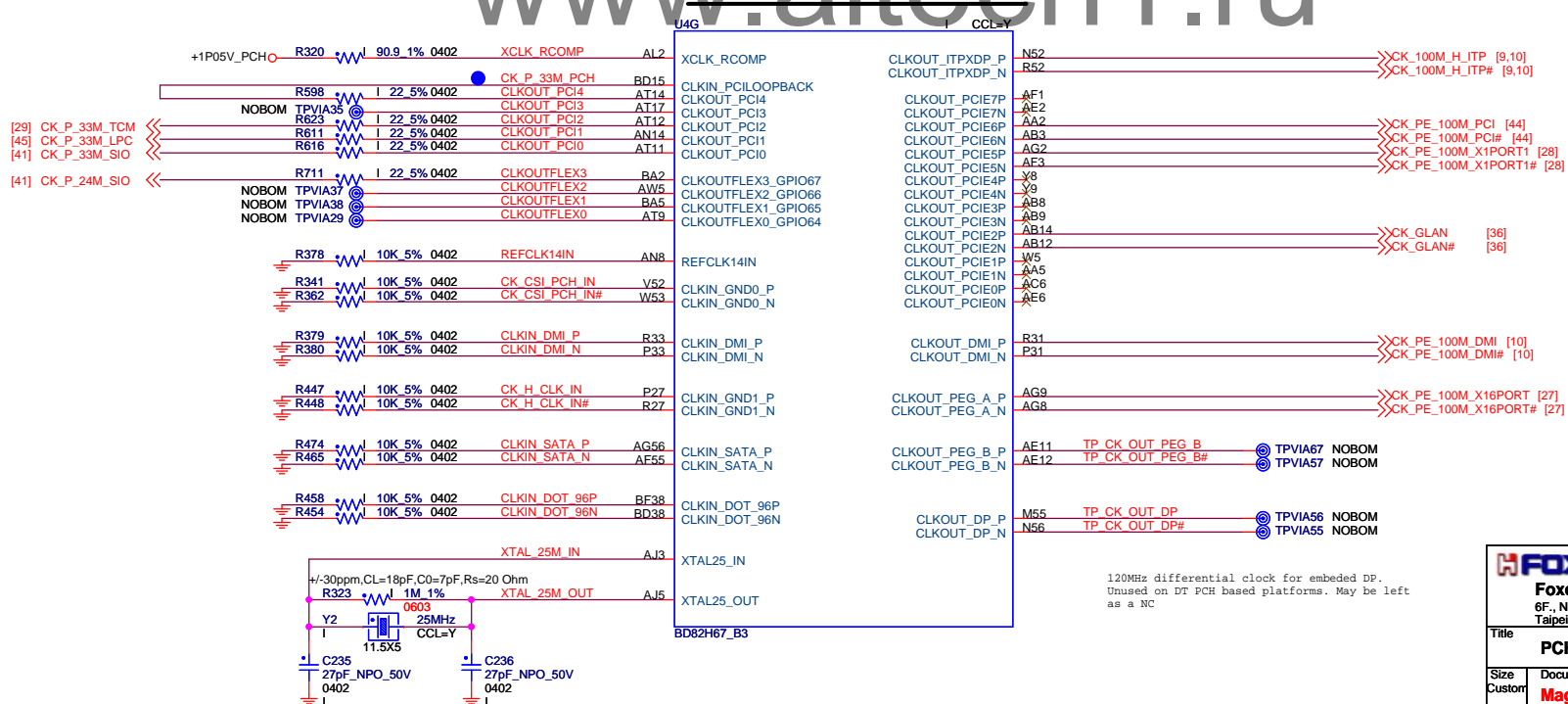
The image displays a complex PCB layout for a Magellan-H67 board. The layout is organized into several functional blocks, each with its own set of components and connections. Key blocks include:

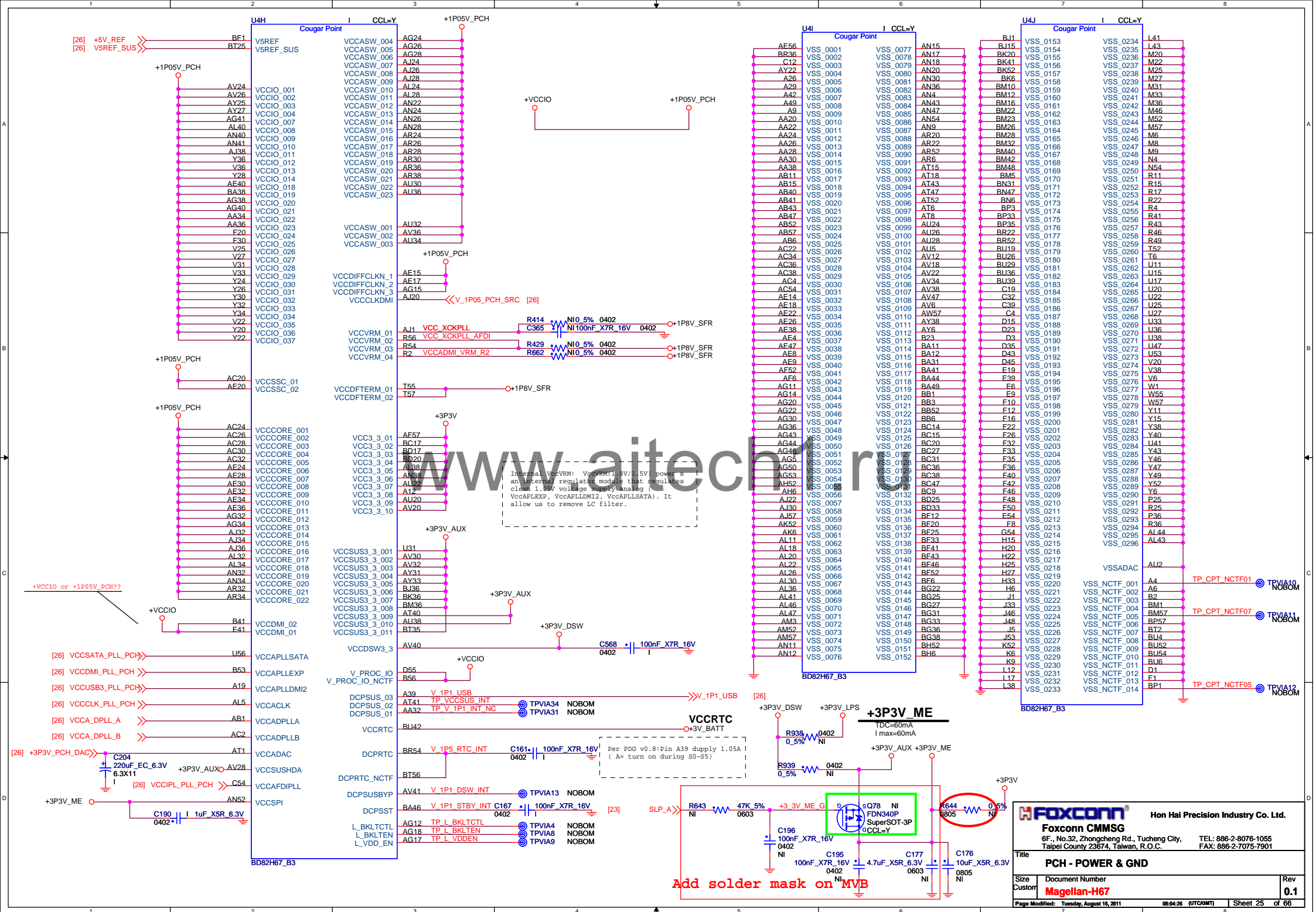
- APWROK:** Contains components like R139, R140, R141, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R281, R282, R283, R284, R285, R286, R287, R288, R289, R290, R291, R292, R293, R294, R295, R296, R297, R298, R299, R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311, R312, R313, R314, R315, R316, R317, R318, R319, R320, R321, R322, R323, R324, R325, R326, R327, R328, R329, R330, R331, R332, R333, R334, R335, R336, R337, R338, R339, R340, R341, R342, R343, R344, R345, R346, R347, R348, R349, R350, R351, R352, R353, R354, R355, R356, R357, R358, R359, R360, R361, R362, R363, R364, R365, R366, R367, R368, R369, R370, R371, R372, R373, R374, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388, R389, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R400, R401, R402, R403, R404, R405, R406, R407, R408, R409, R410, R411, R412, R413, R414, R415, R416, R417, R418, R419, R420, R421, R422, R423, R424, R425, R426, R427, R428, R429, R430, R431, R432, R433, R434, R435, R436, R437, R438, R439, R440, R441, R442, R443, R444, R445, R446, R447, R448, R449, R450, R451, R452, R453, R454, R455, R456, R457, R458, R459, R460, R461, R462, R463, R464, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804, R805, R806, R807, R808, R809, R810, R811, R812, R813, R814, R815, R816, R817, R818, R819, R820, R821, R822, R823, R824, R825, R826, R827, R828, R829, R830, R831, R832, R833, R834, R835, R836, R837, R838, R839, R840, R841, R842, R843, R844, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900, R901, R902, R903, R904, R905, R906, R907, R908, R909, R910, R911, R912, R913, R914, R915, R916, R917, R918, R919, R920, R921, R922, R923, R924, R925, R926, R927, R928

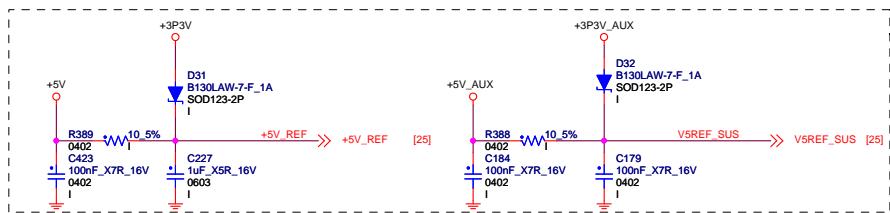
PCH - DP AND FDI



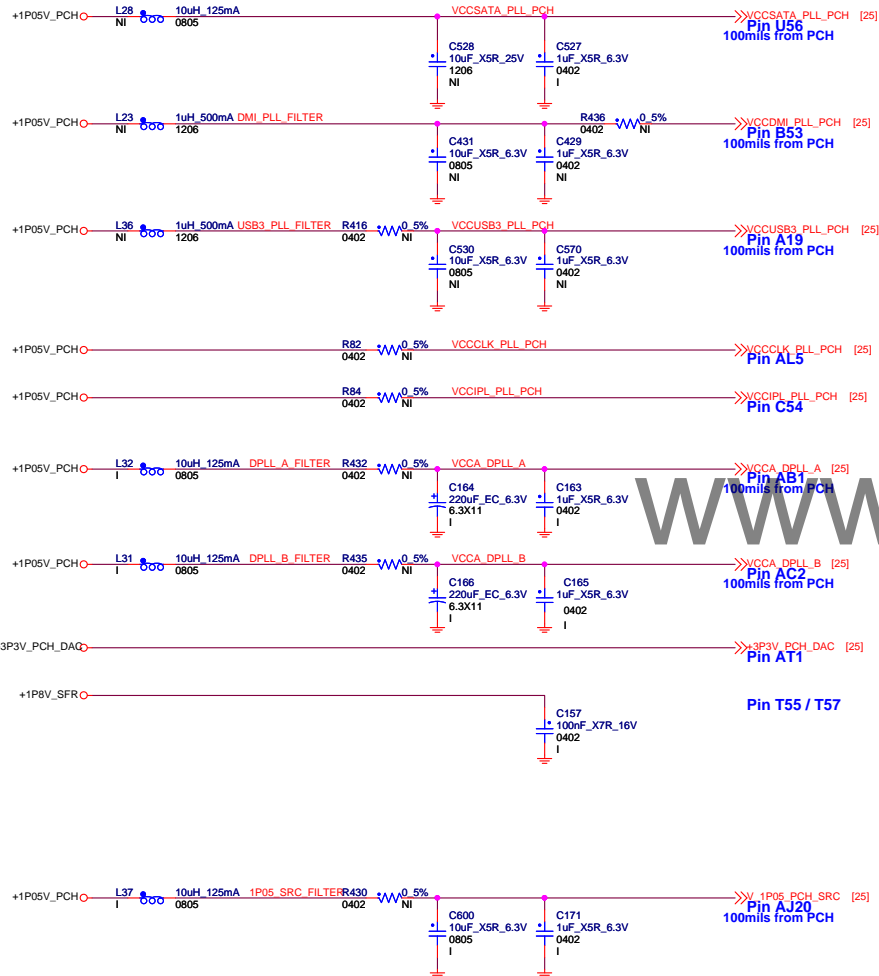
PCH - CLOCK DISTRIBUTION



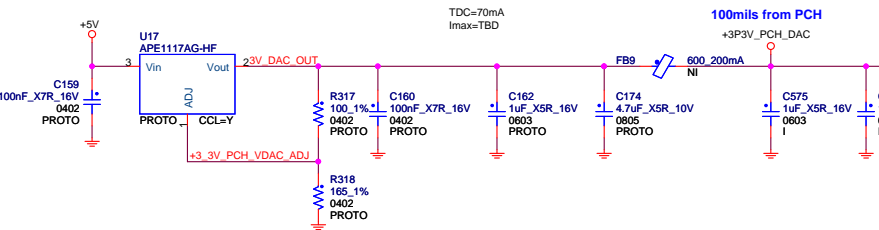




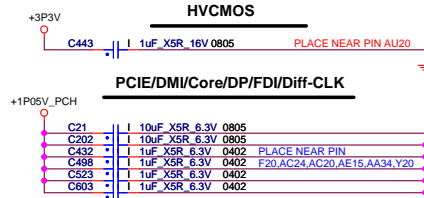
FILTER



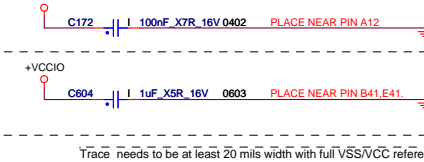
+3_3V_PCH_DAC



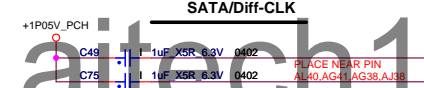
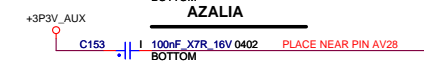
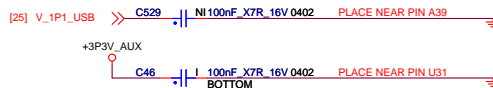
Maybe can del the D31/D32, Follow PDG 2.0, Sequence only For "M"



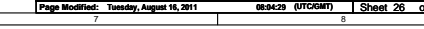
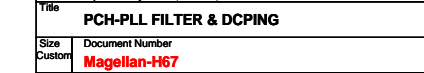
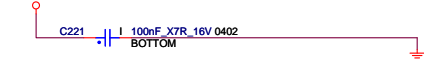
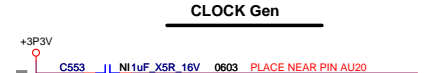
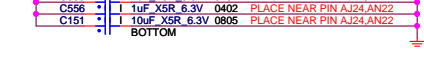
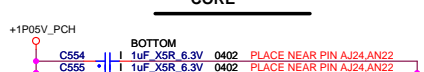
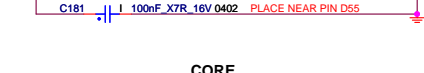
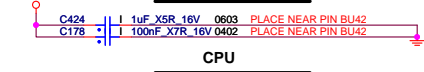
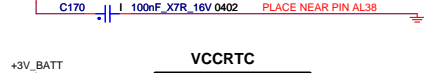
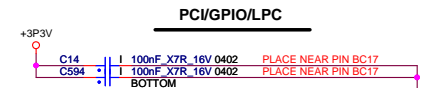
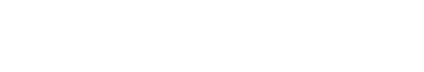
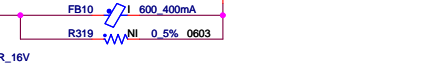
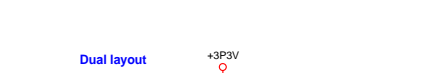
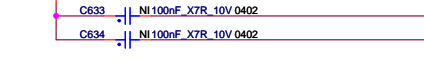
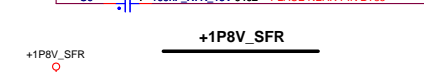
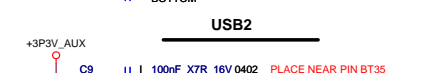
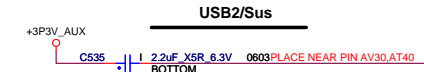
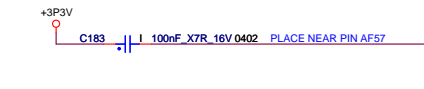
PCIE/DMI/Core/DP/FDI/Diff-CLK



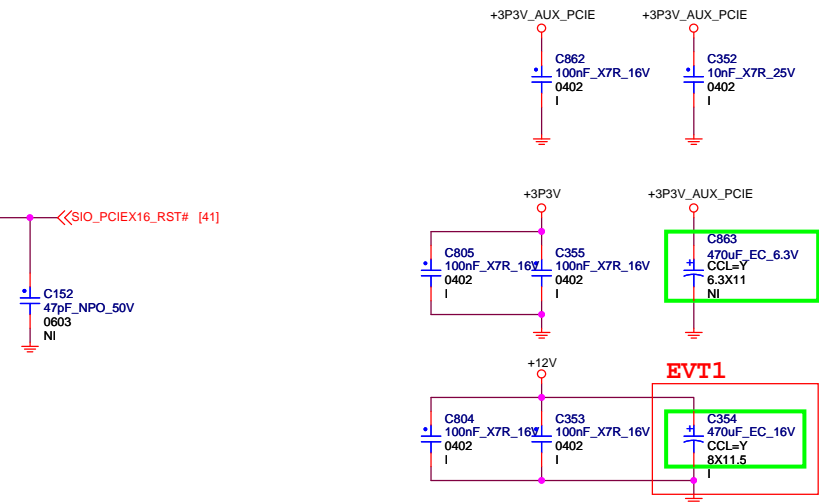
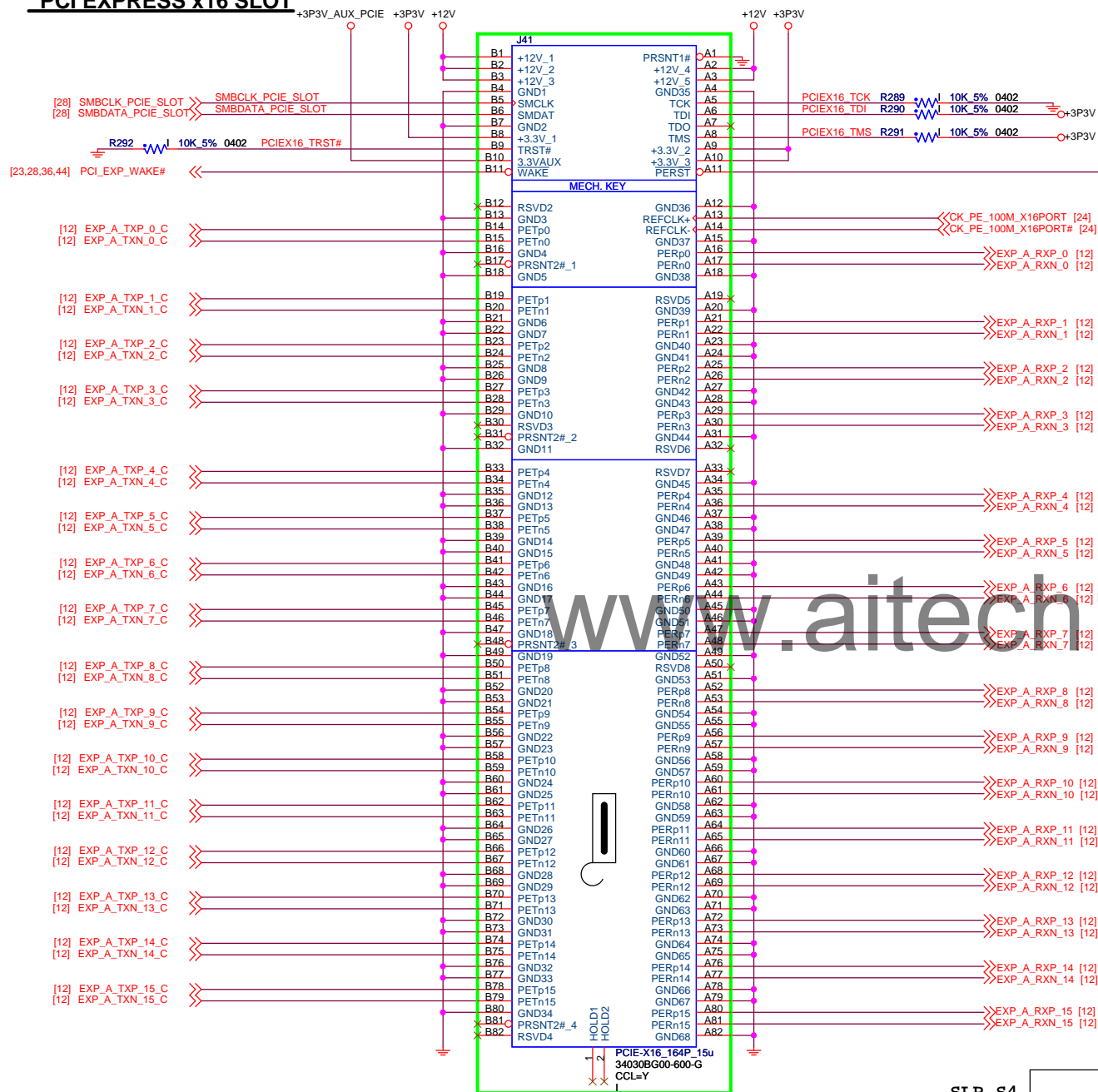
USB 3



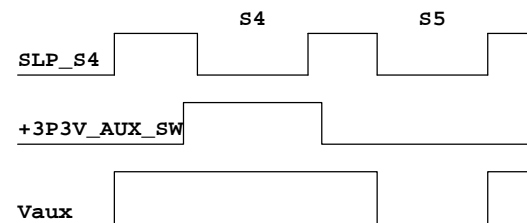
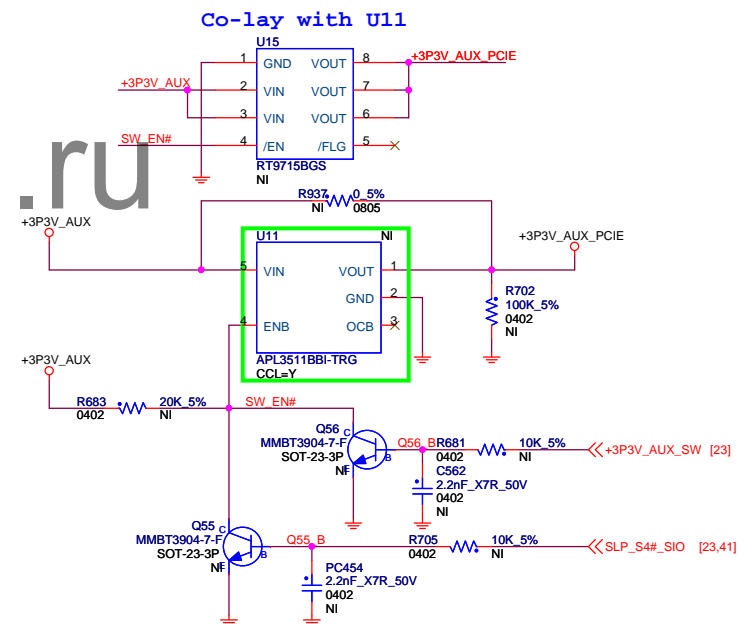
SATA



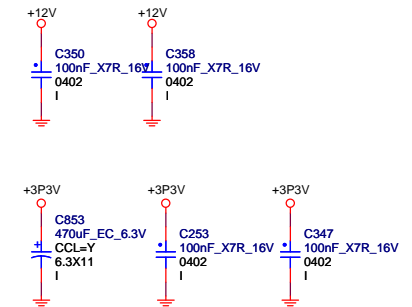
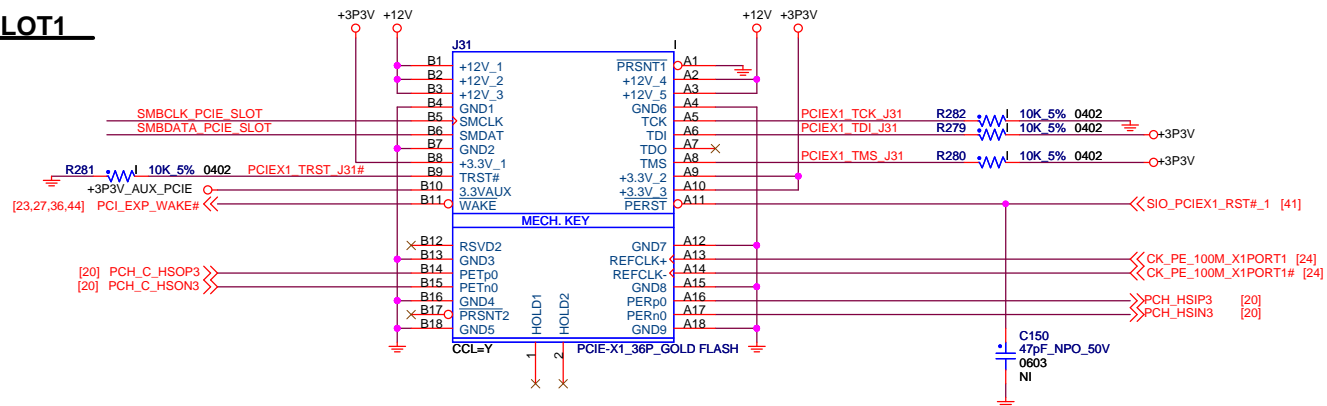
PCI EXPRESS x16 SLOT



1. Remove U11 and related parts on PVT
2. Connect +3P3V_AUX and +3P3V_AUX_PCIE directly

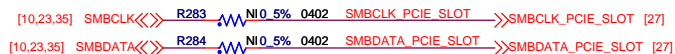


PCI EXPRESS X1 SLOT1

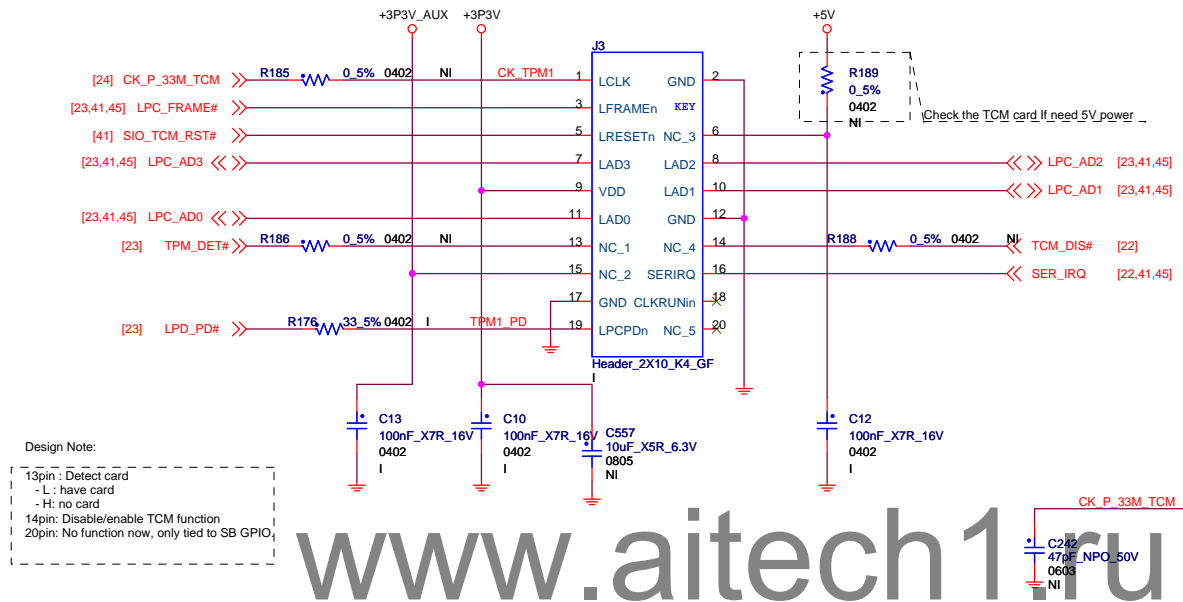


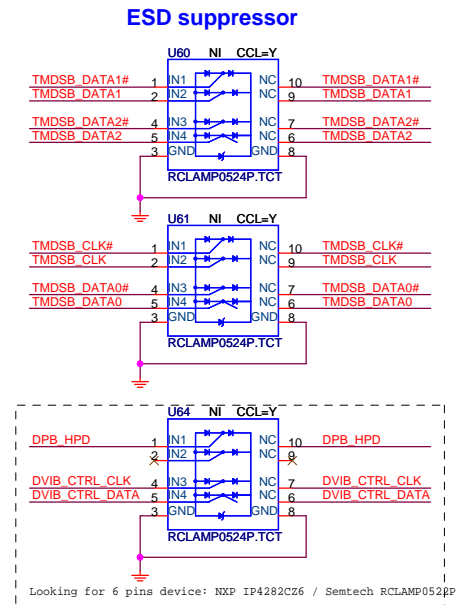
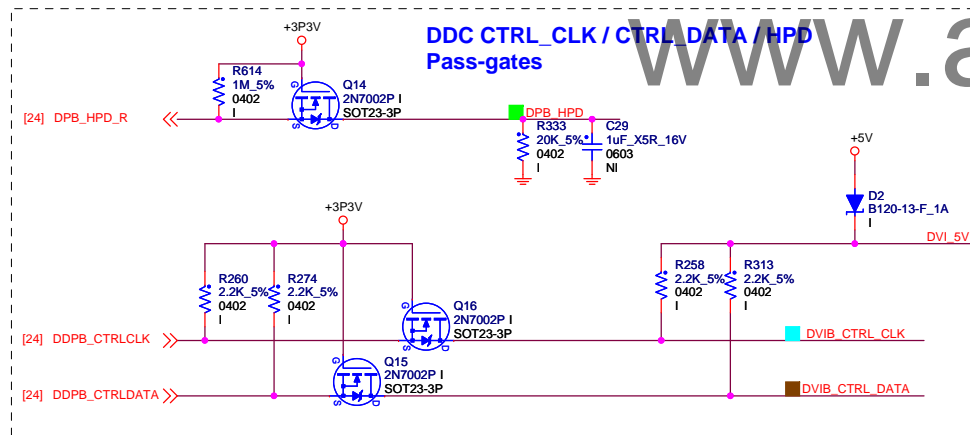
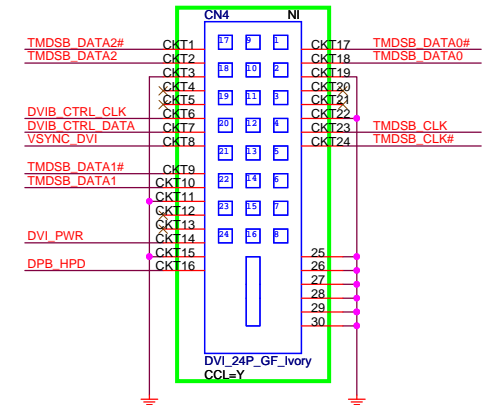
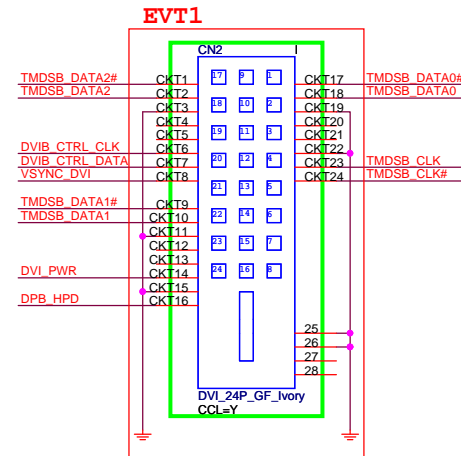
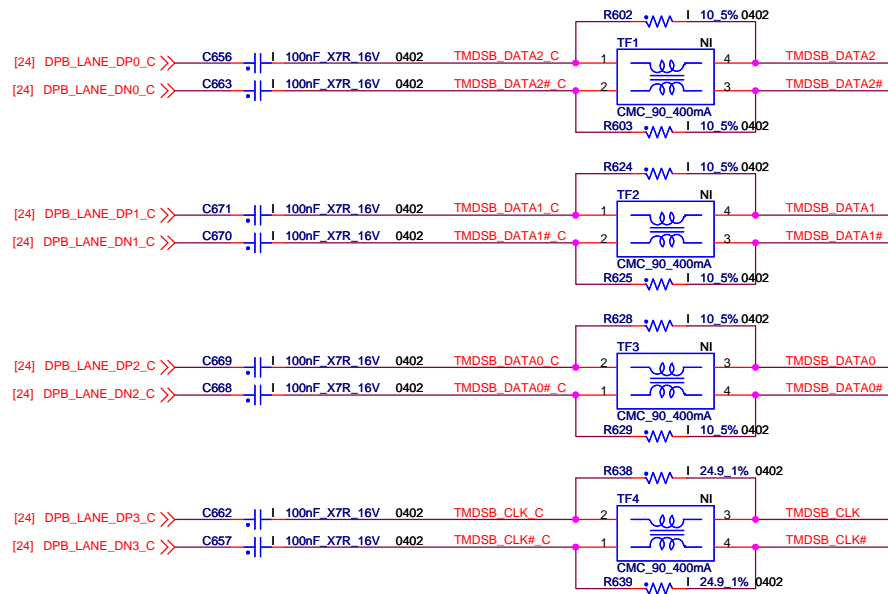
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For Monotonic improve use

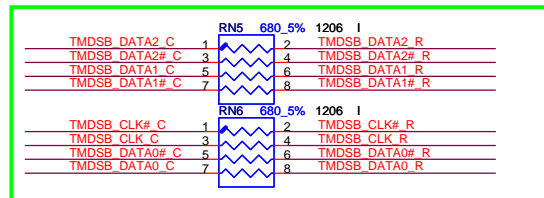


TCM Header

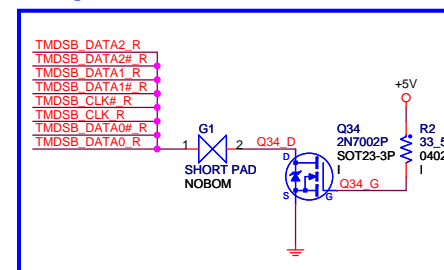


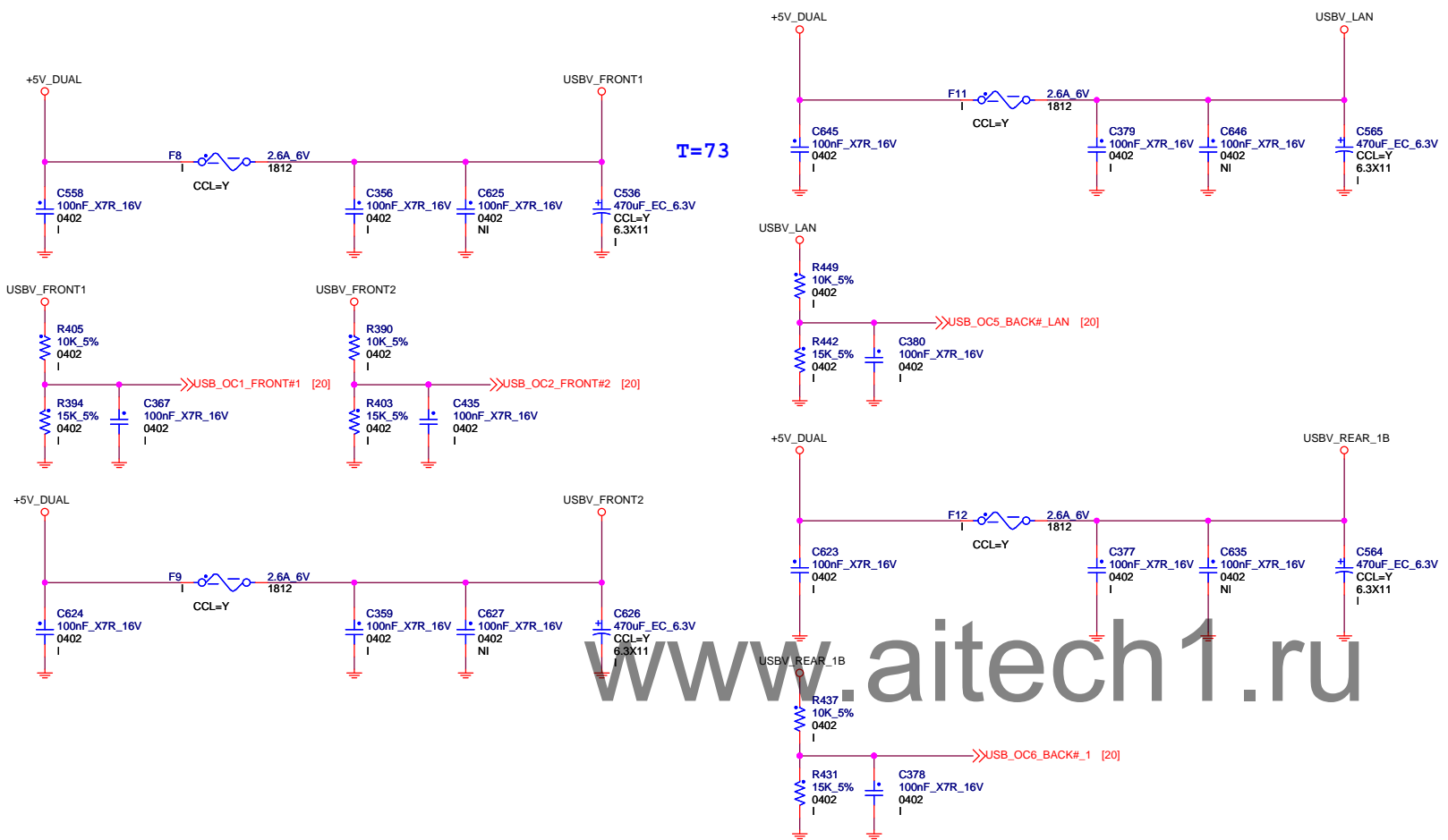


Cost Reduced Level Shifter Solution

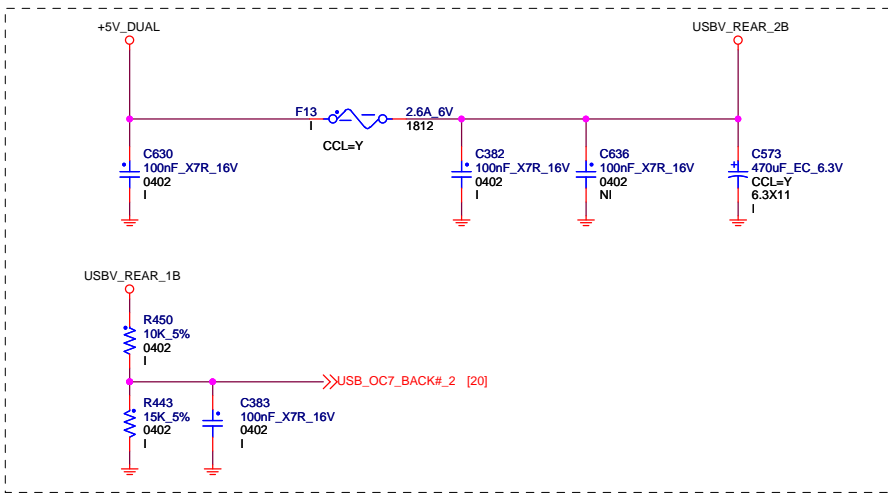


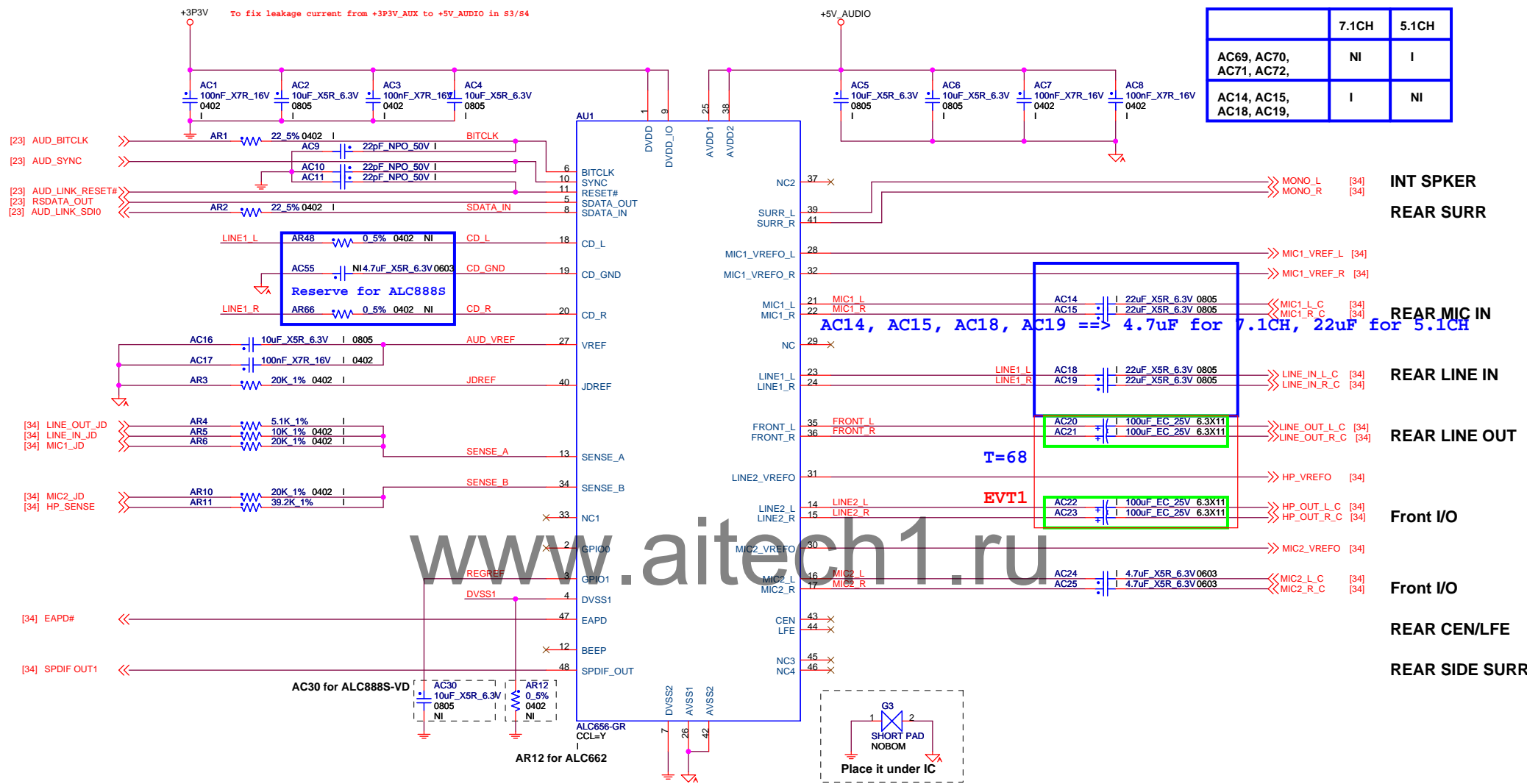
Co-layout with U6



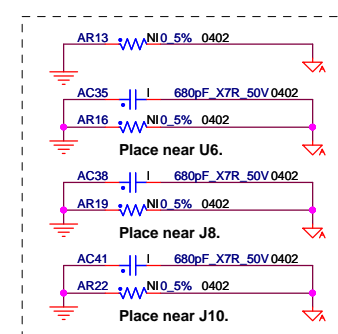
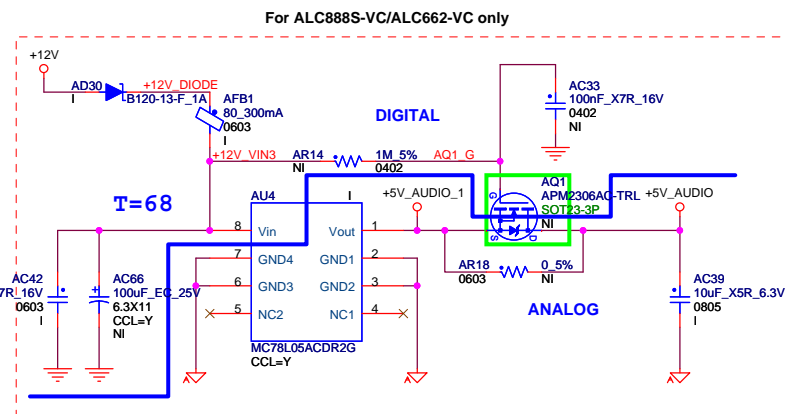


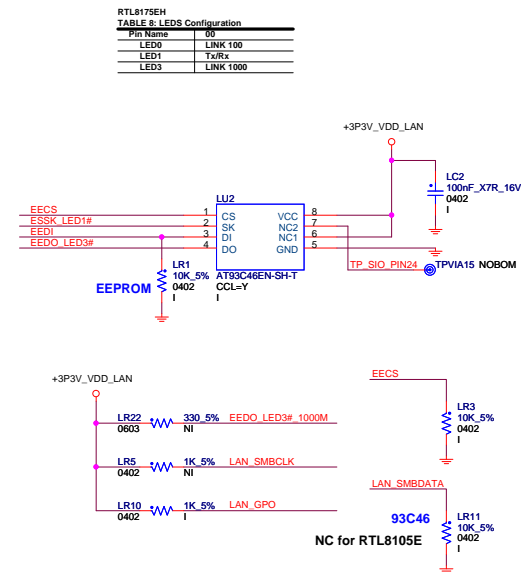
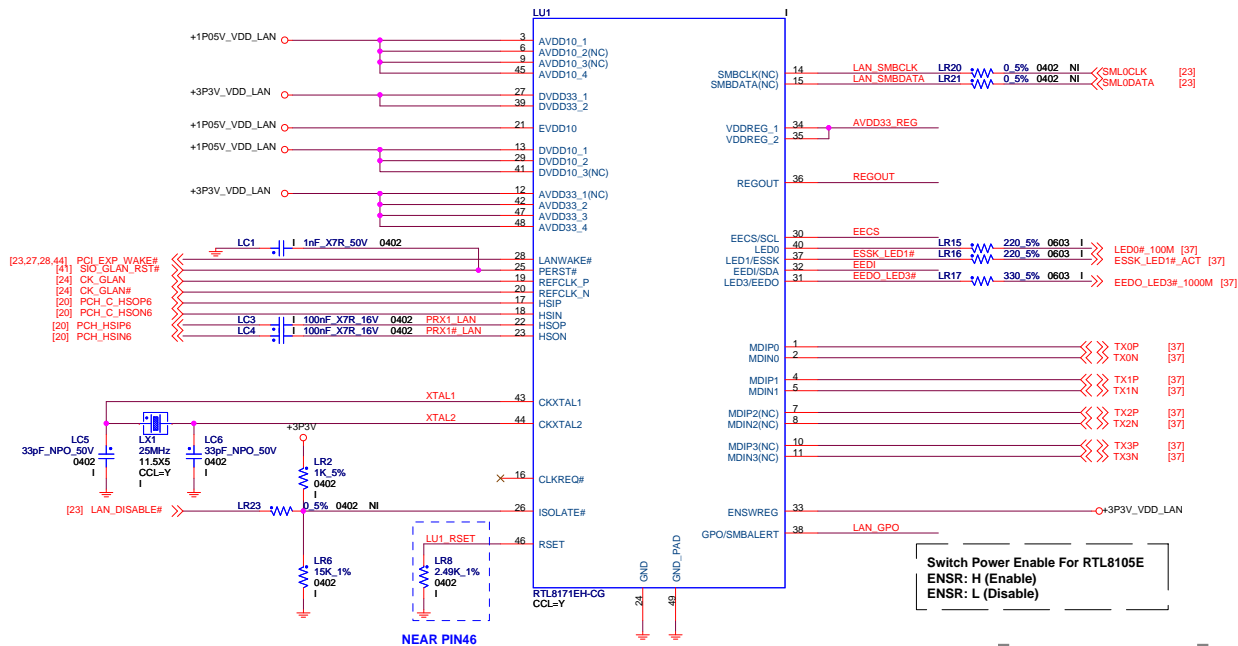
Add USB_REAR_2B power for increase two rear USB ports (USB_12, USB_13)





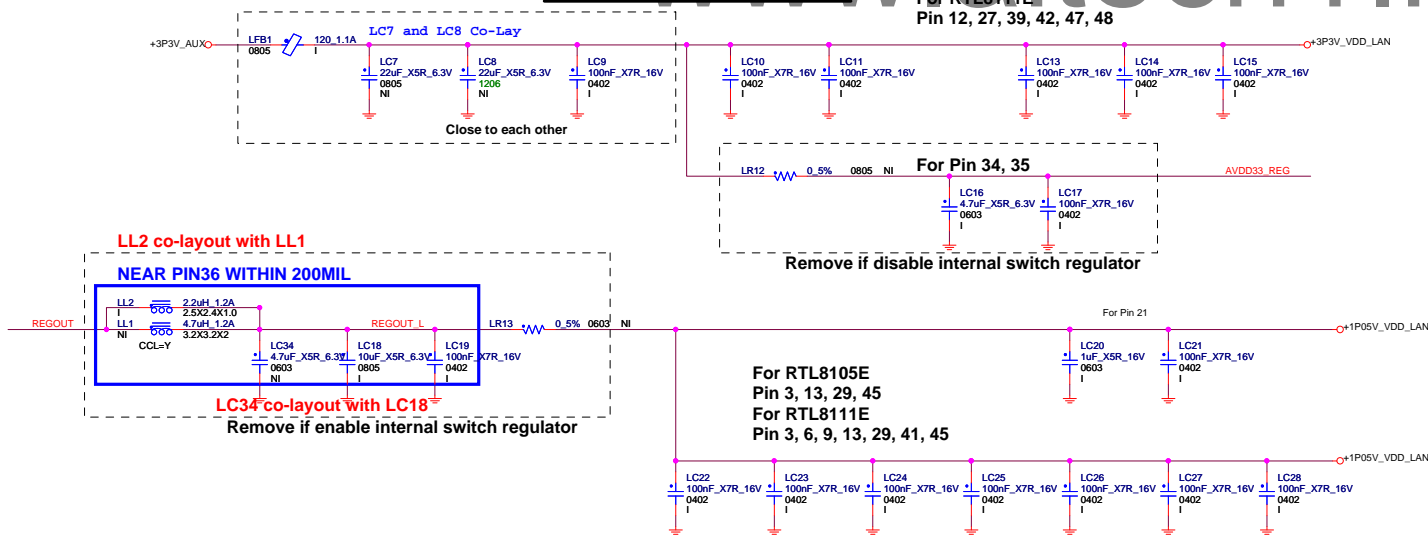
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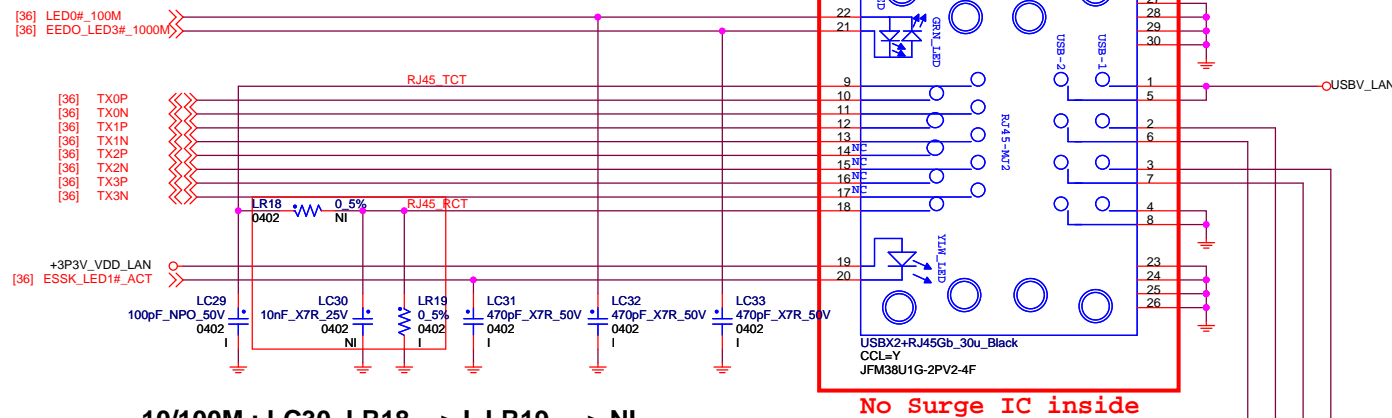
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For RTL8105E
Pin 27, 39, 42, 47, 48
For RTL8111E
Pin 12, 27, 39, 42, 47, 48



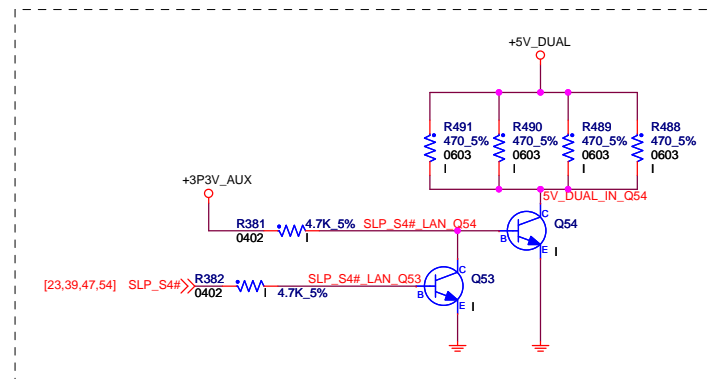
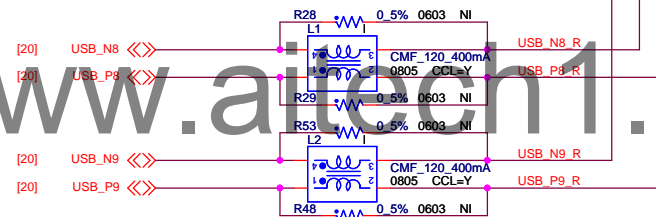
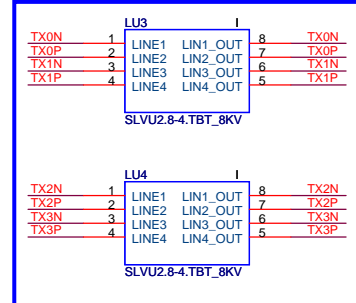
REAR LAN + USB

Ports 12 & 13

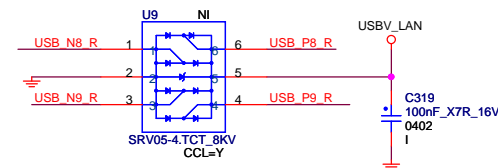


10/100M : LC30, LR18==> I, LR19 ==> NI
1000M : LC30, LR18 ==> NI, LR19 ==> I

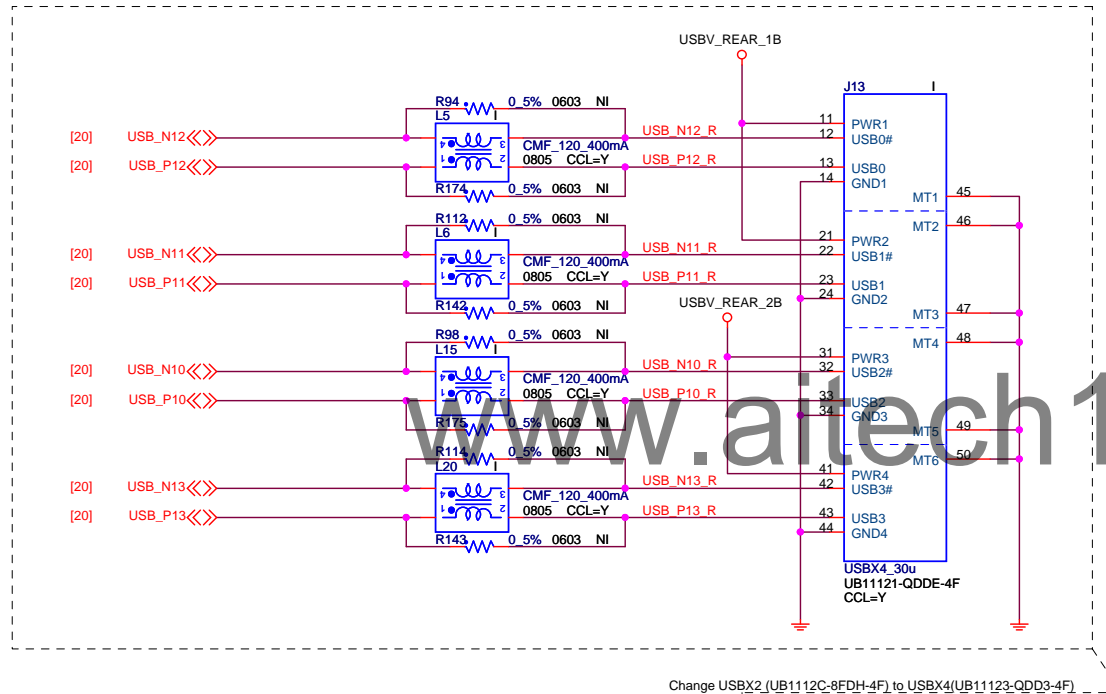
Surge IC close to RJ45



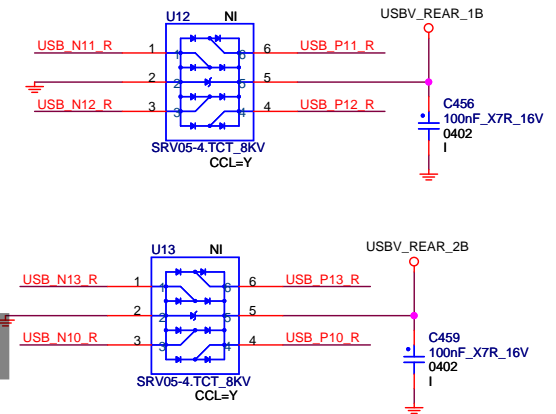
LAN USB ESD Component

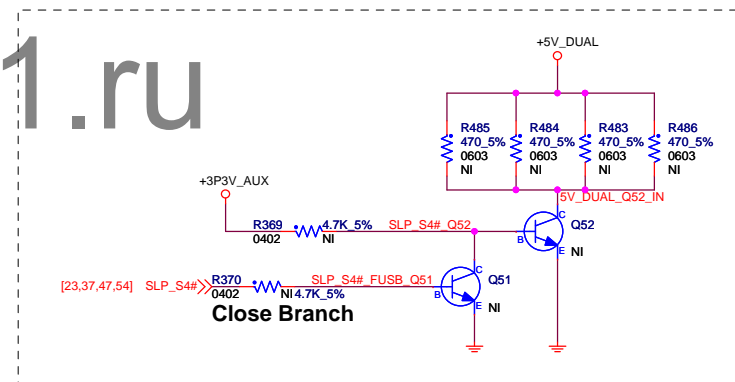
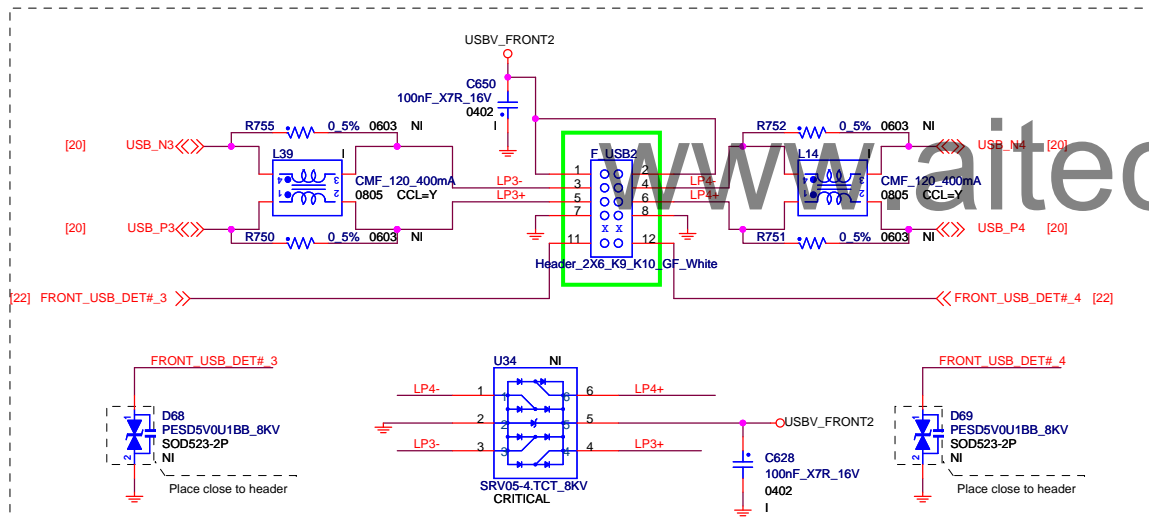
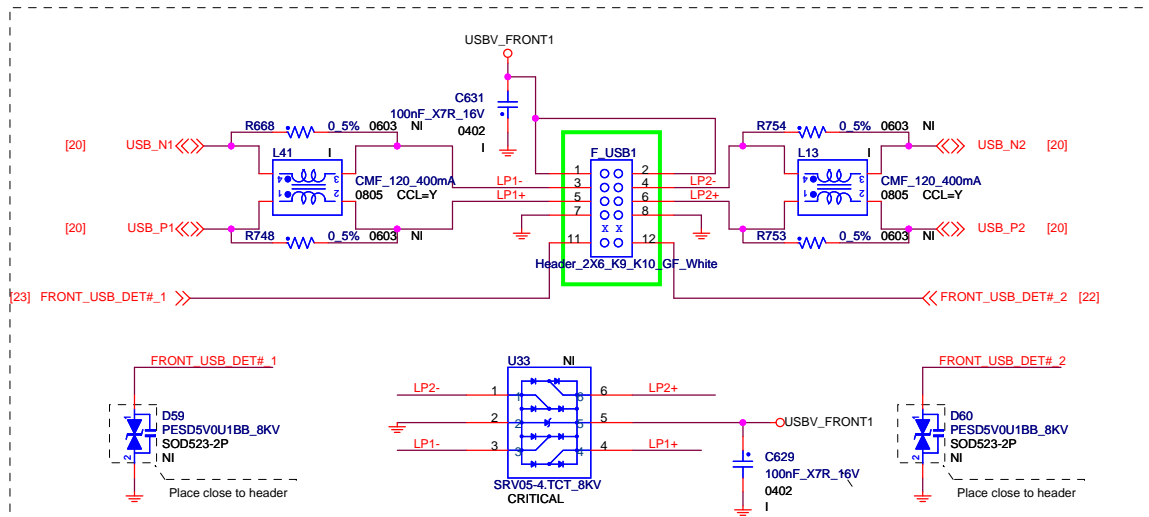


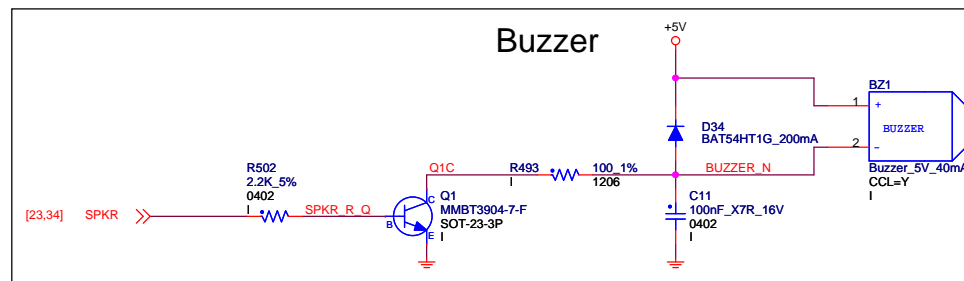
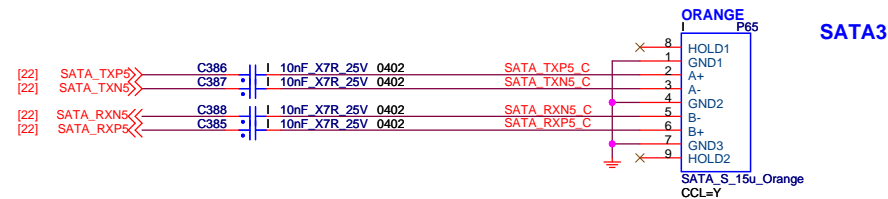
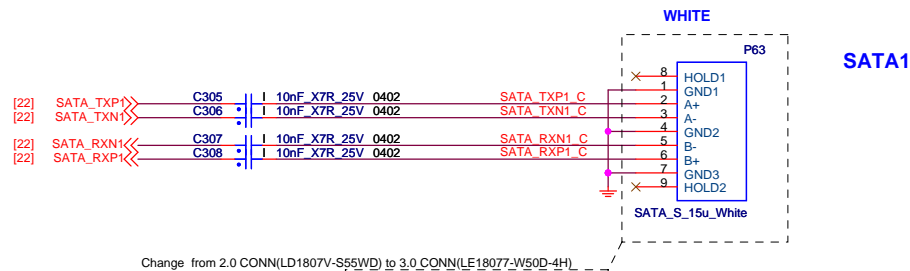
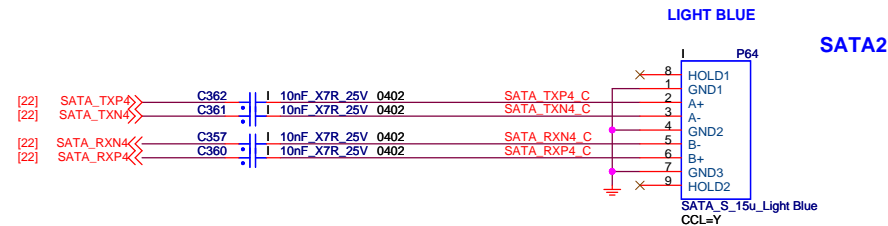
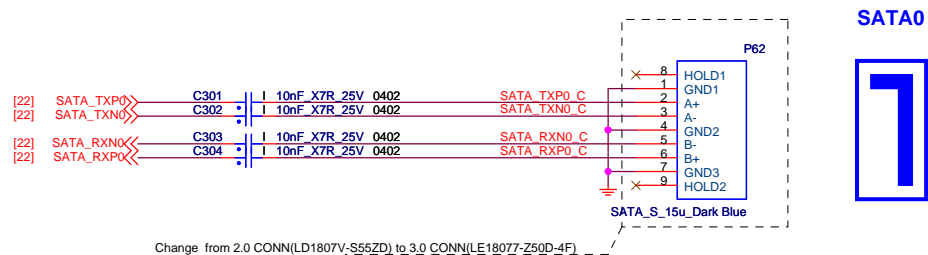
REAR USB



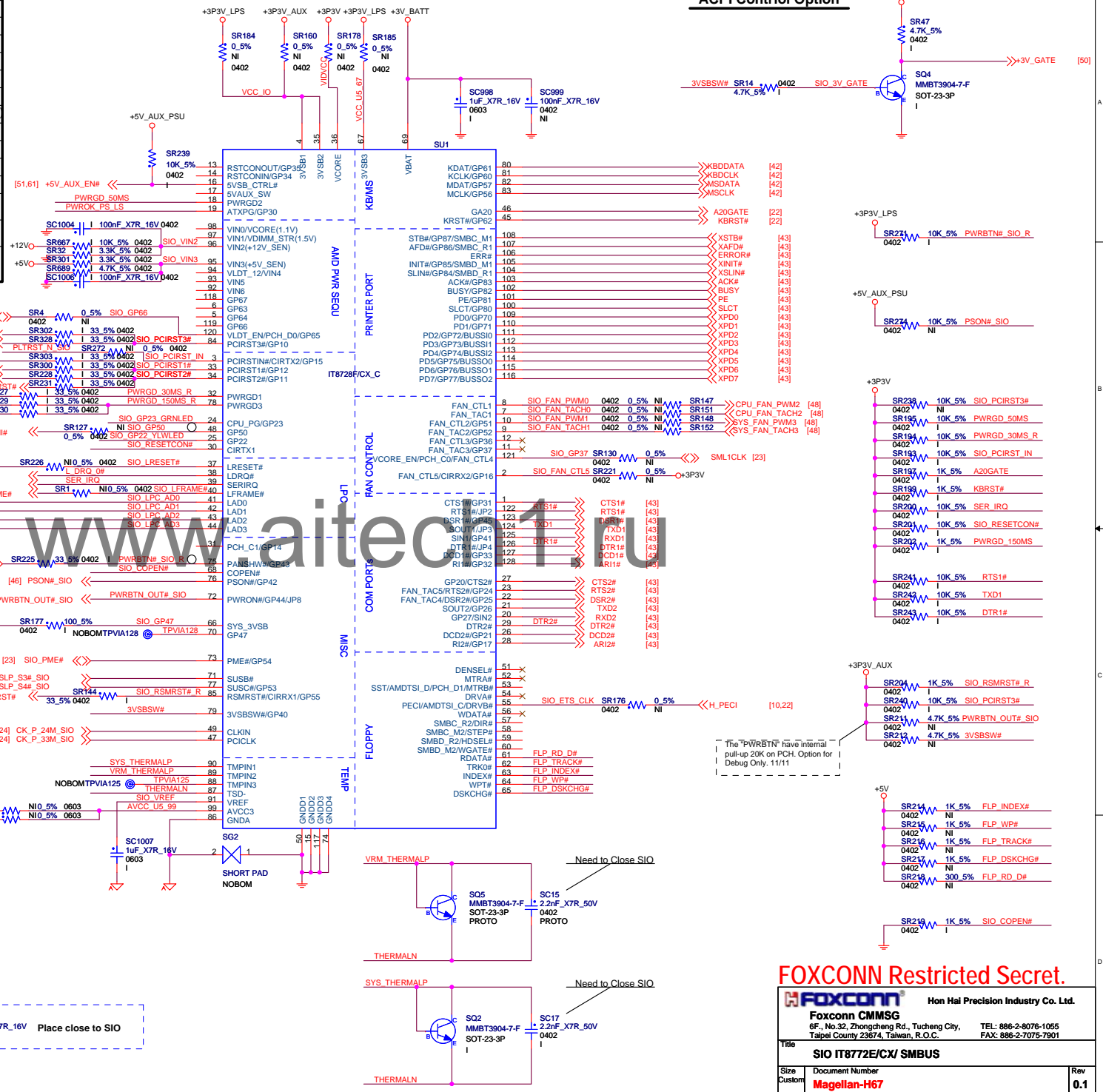
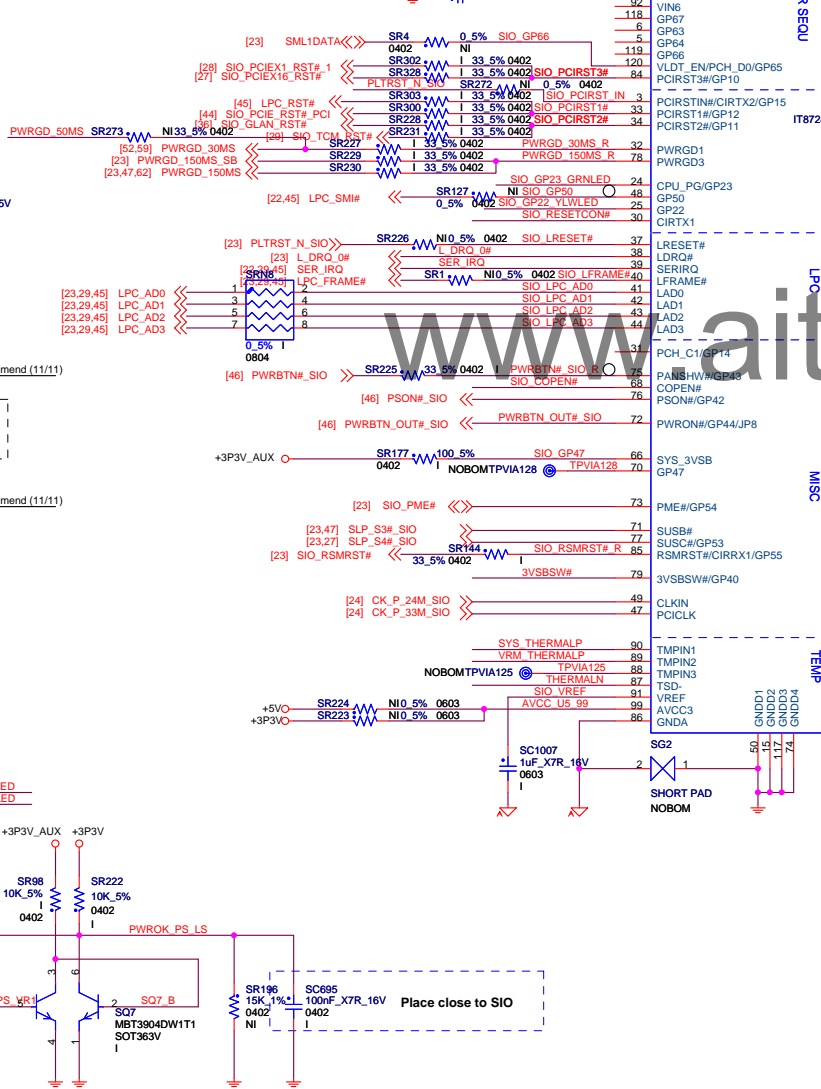
REAR USB ESD Component






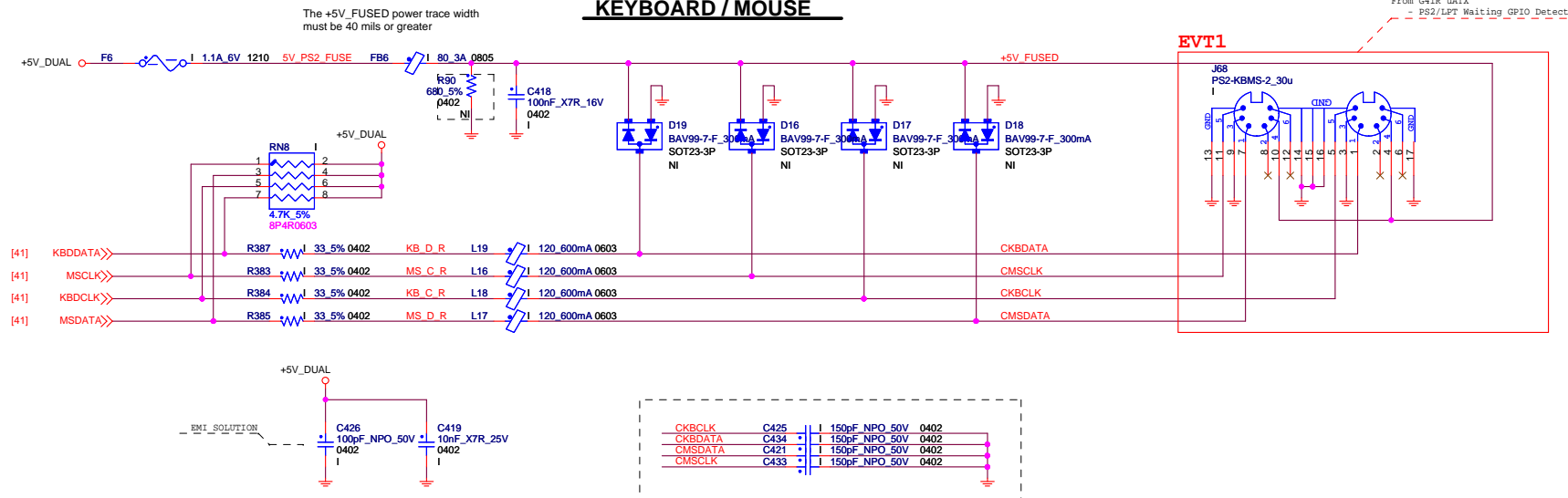


Symbol	value	Description
JP3	1	Disabled.
Flashseg1_EN	0	Flash I/F Address Segment 1 is enabled
JP4	1	K8 power sequence function is disabled
K8PWR_EN	0	K8 power sequence function is enabled
JP3 & JP5	11	The default value of EC Index 15h/16h/17h is 40h
FAN_CTL_SEL	01	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
Pin 124 & 46	01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
	00	The default value of EC Index 15h/16h/17h is 20h
JP5	1	Disable WDT to rest PWROK
WDT_EN	0	Enable WDT to rest PWROK
JP2/JP6	11	Disable VID/SVID out pins
SVID_EN	01	For Intel Platform Enable VIDO0-VIDO7 output pins.
Pin122/Pin29	10	For AMD Platform(always serial output) Enable SVD(Pin3)/SVC(Pin31)Output pins
	00	For AMD Platform(Serial-IN/Serial-Out and Parallel-IN/Parallel-Out it is selected by CPU)



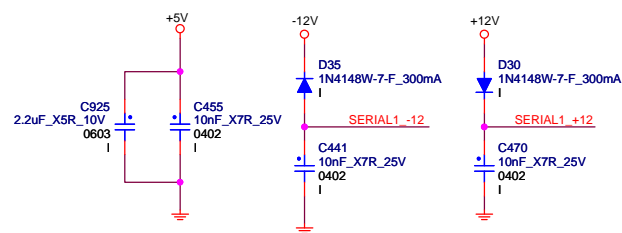
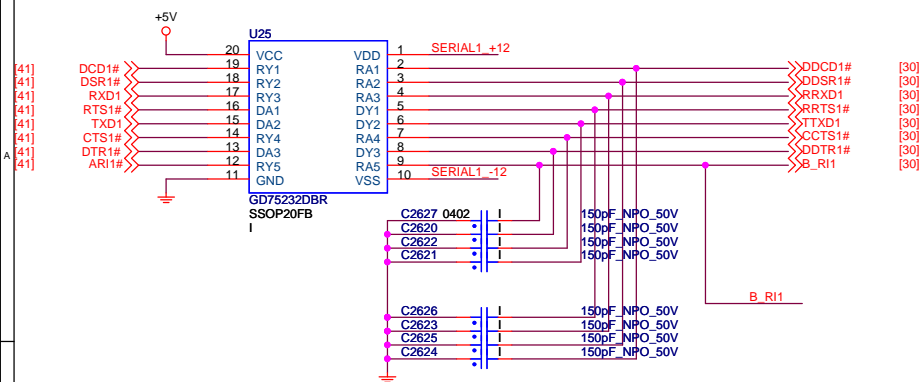
		FOXCONN Restricted Secret.	
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Foxconn CHONGSG 6F., No.32, Zhongxing Rd., Tucheng City, Taipei County 23674, Taiwan, R.O.C.		TEL: 886-2-806-1055 FAX: 886-2-7075-7901	
Title	SIO IT8772E/CX/ SMBUS		
Size Custom	Document number Magellan-H67		Rev 0
Page Modified: Tuesday, August 16, 2011		06:04:30 (UTC+GMT)	Sheet 41 of 60

KEYBOARD / MOUSE

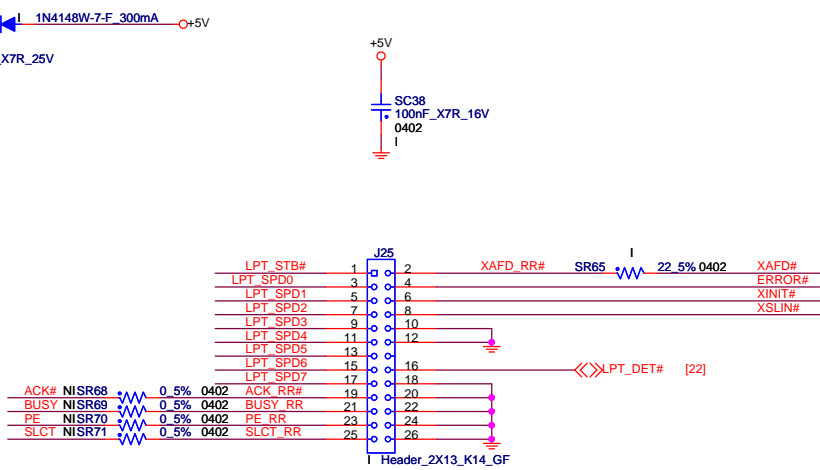
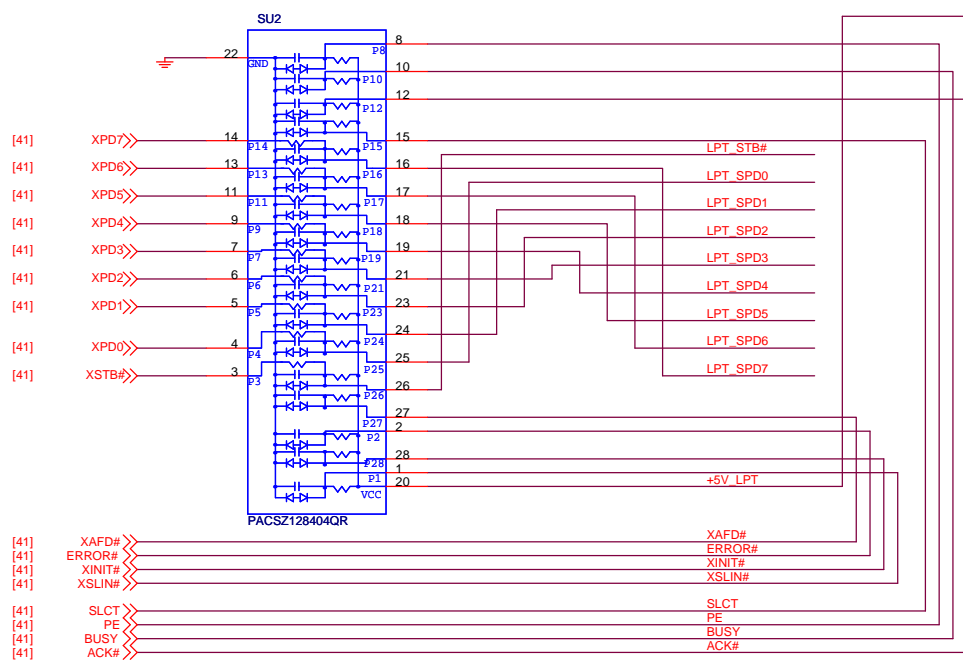
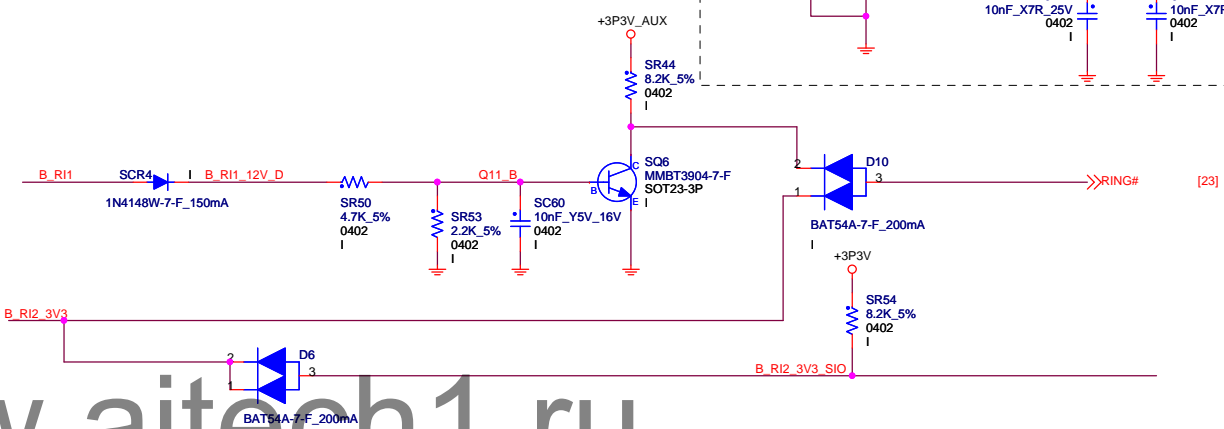
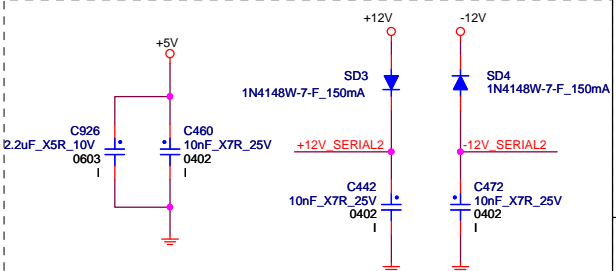
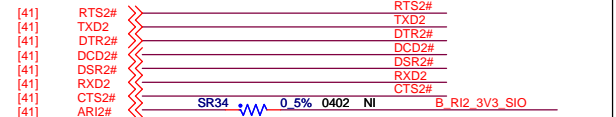
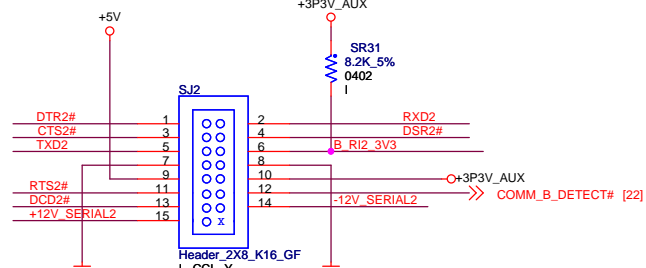


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COM1



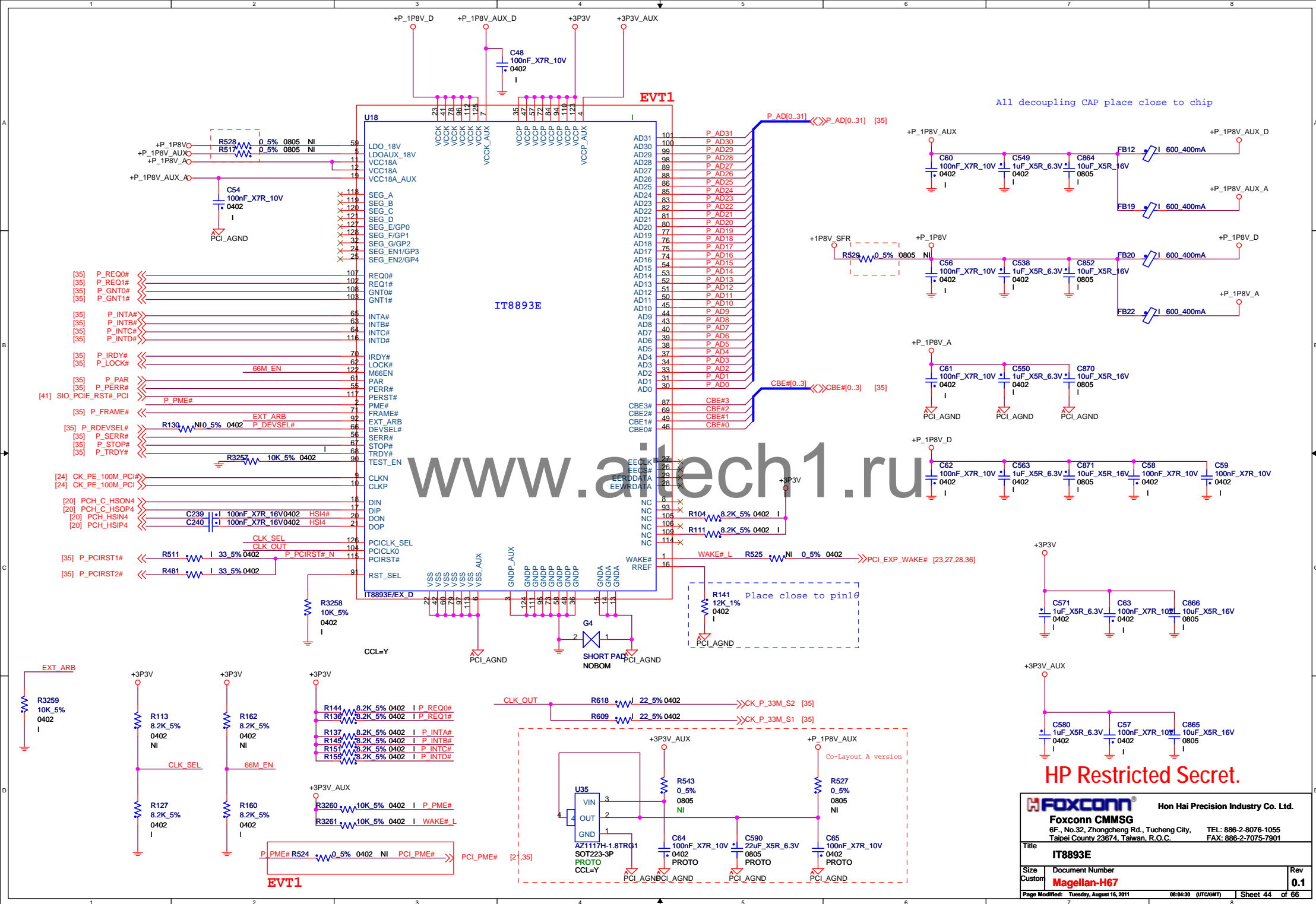
COM2 Header



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Title			
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Size	Document Number		
Custom	Magellan-H67		
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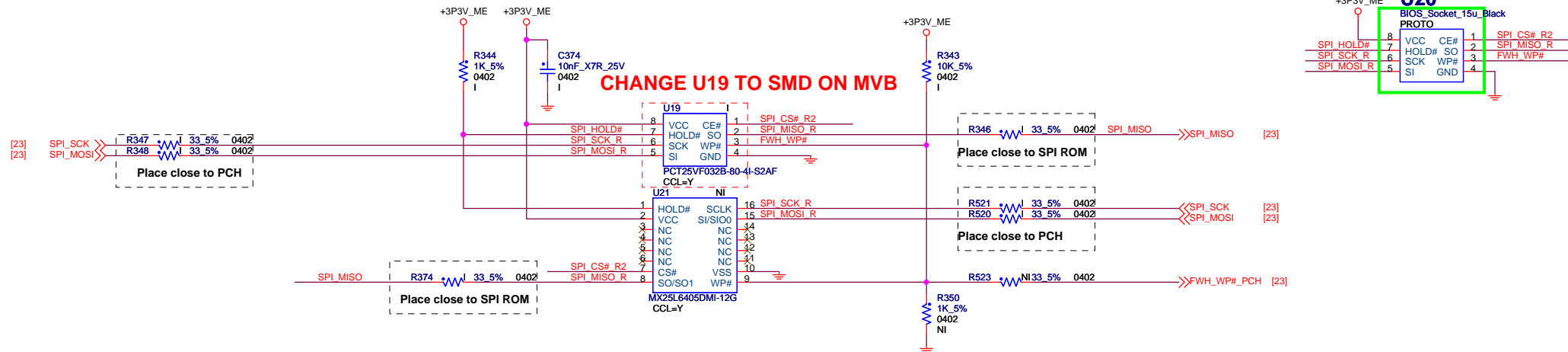
Foxconn GMMSG

6F., No.32, Zhongcheng Rd., Tucheng City,
Taipei County 23674, Taiwan, R.O.C.

Title		IT8893E	
Size	Document Number	F	
Custom	Magellan-H67	F	
Page Modified: Tuesday, August 16, 2011		08:04:30 (UTC/GMT)	Sheet 44 of 6

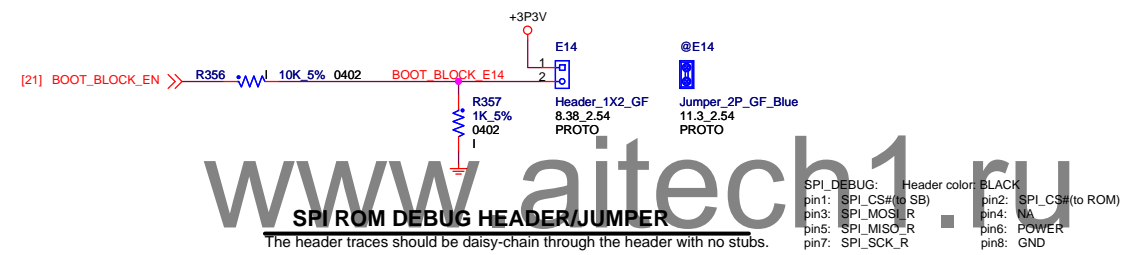
SPI ROM

8 PIN AND 16 PIN SHOULD BE DUAL FOOTPRINT

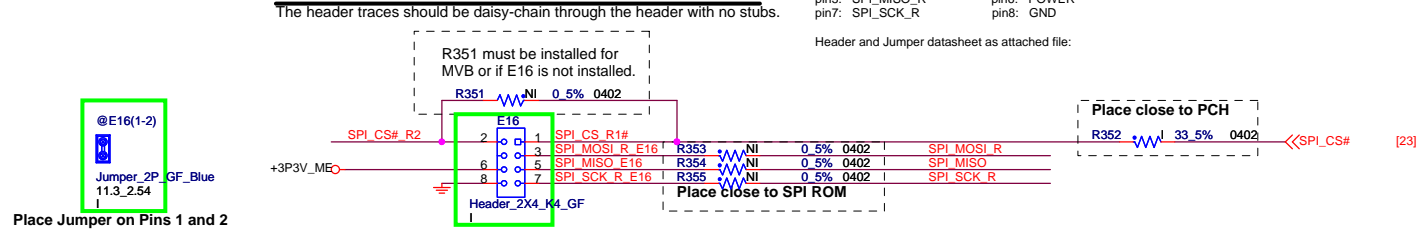


SPI ROM BOOTBLOCK HEADER

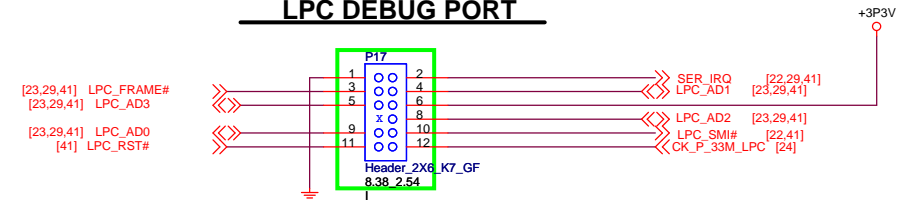
Close SPI ROM



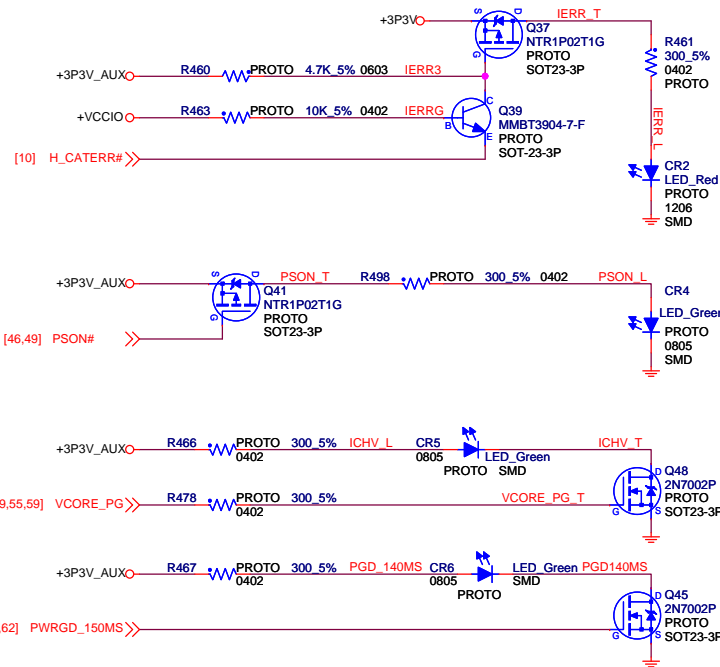
SPI ROM DEBUG HEADER/JUMPER



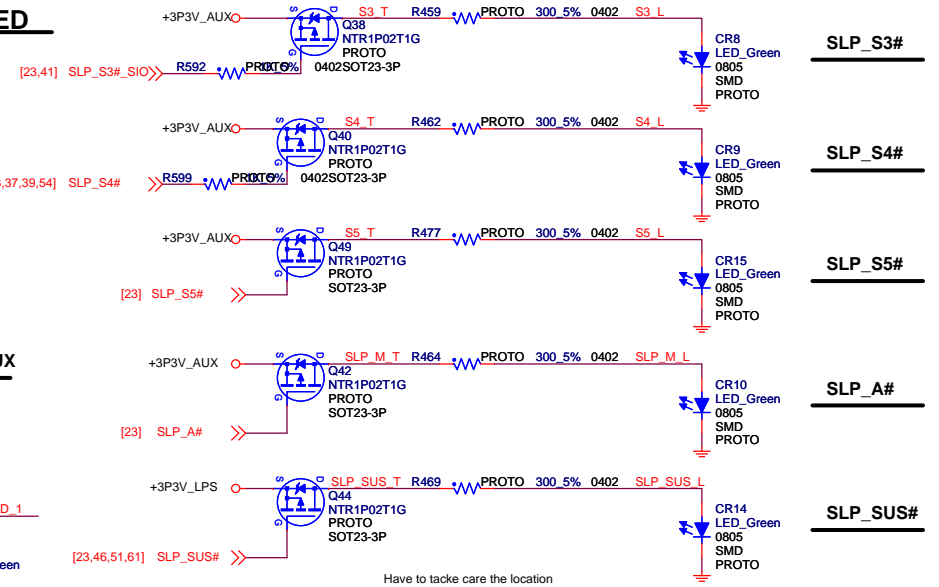
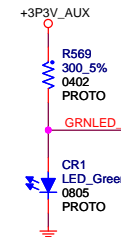
LPC DEBUG PORT



PCA LED



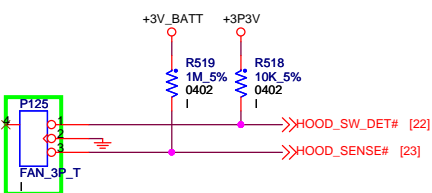
+3P3V_AUX



EVT1

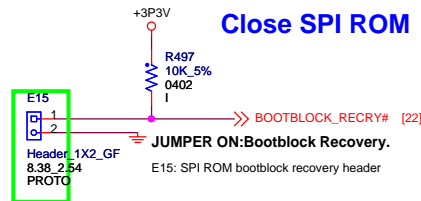
HOOD SENSE CIRCUIT

Have to take care the location

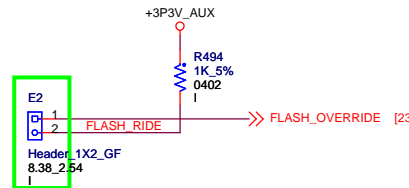


BOOT BLOCK RECOVERY

Close SPI ROM

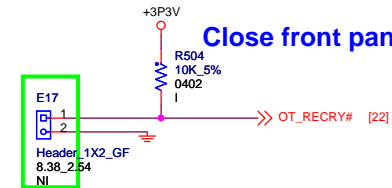


FLASH OVERRIDE



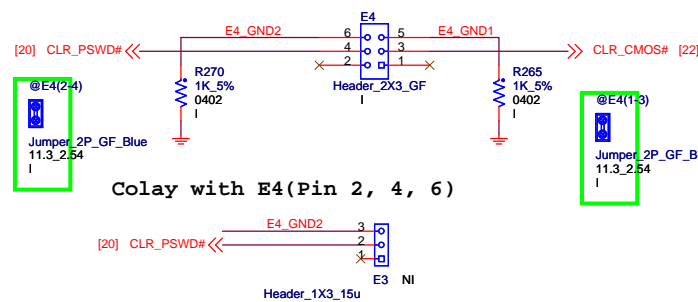
ONE TOUCH RECOVERY

Close front panel



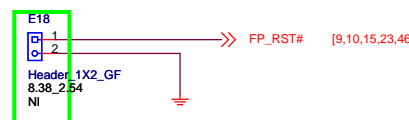
CLEAR PASSWORD

CLEAR CMOS

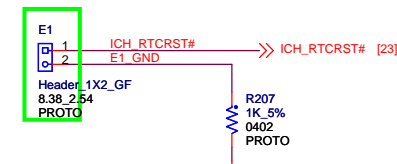


ONE TOUCH RESET

Close front panel

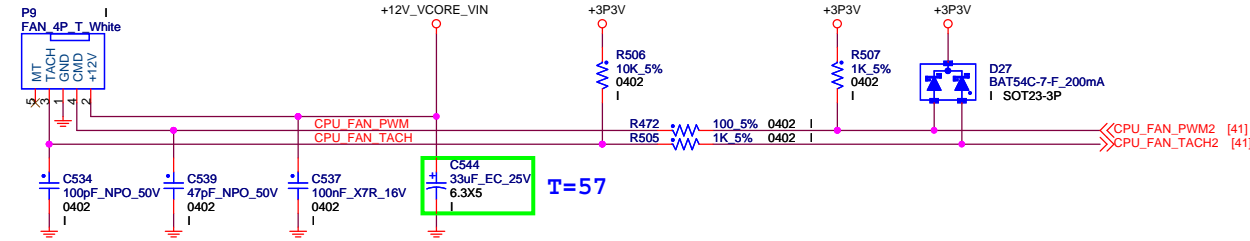


DISCHARGE CMOS



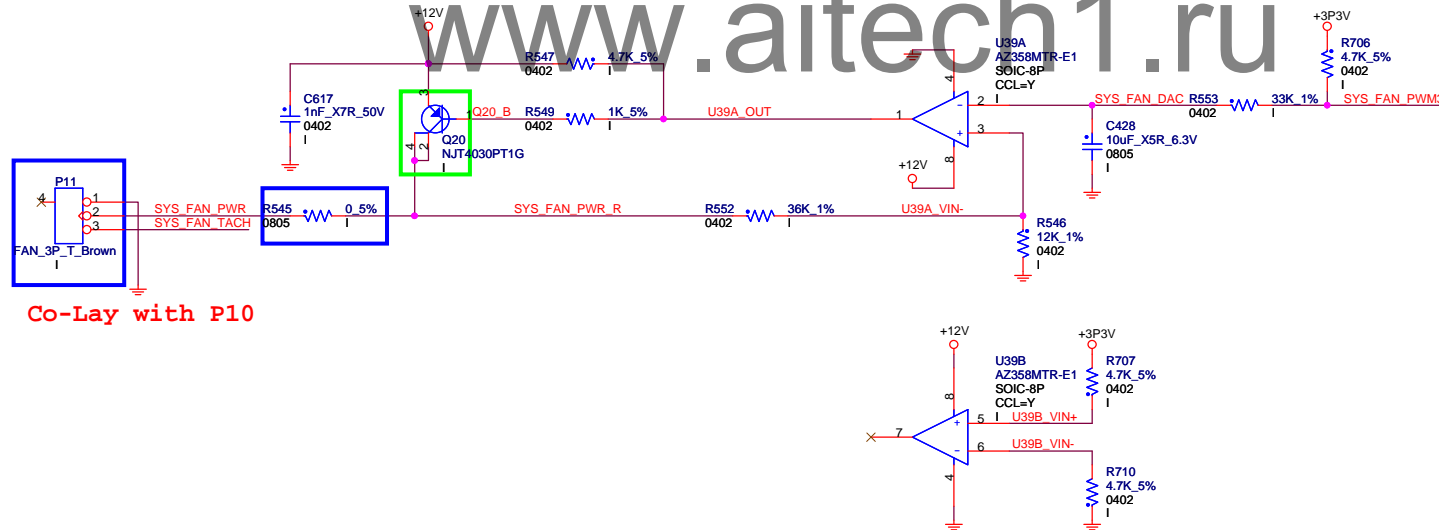
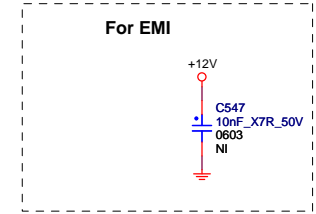
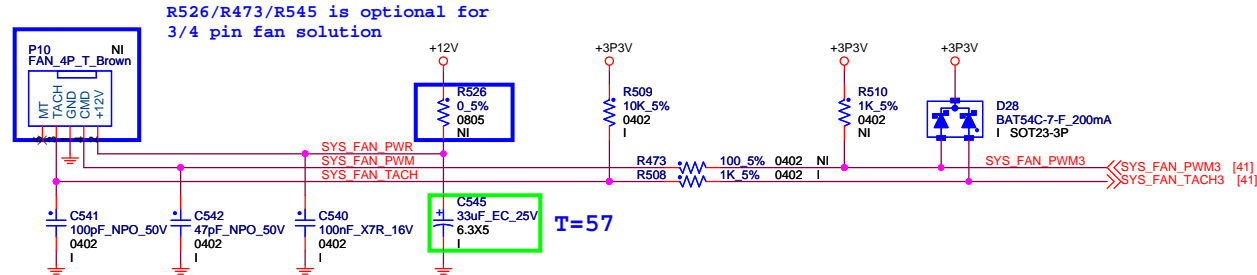
CPU FAN

Color: Brown



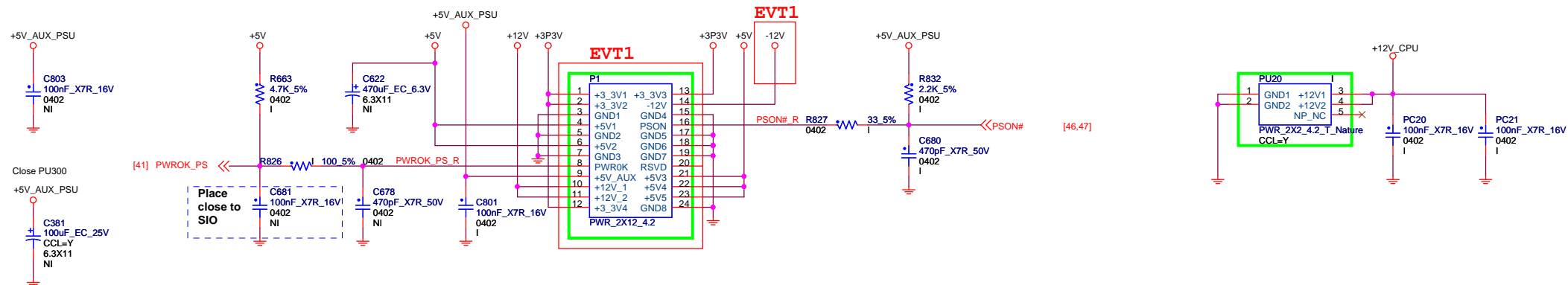
SYSTEM FAN

Color: White



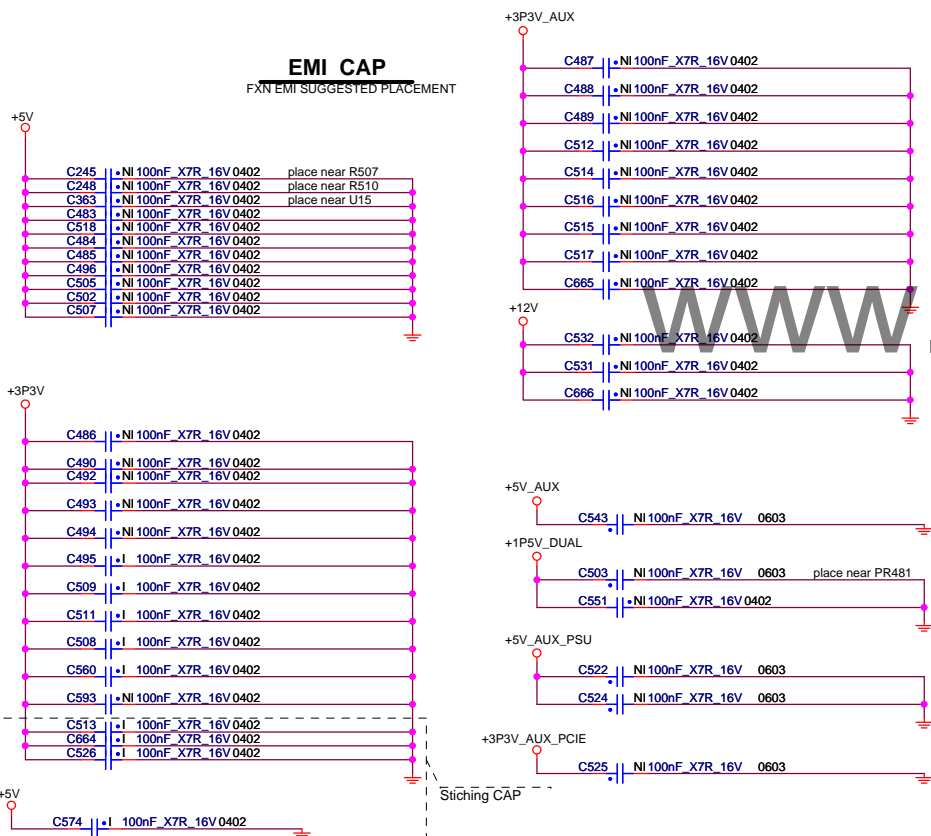
Co-Lay with P10

Power Input Connector



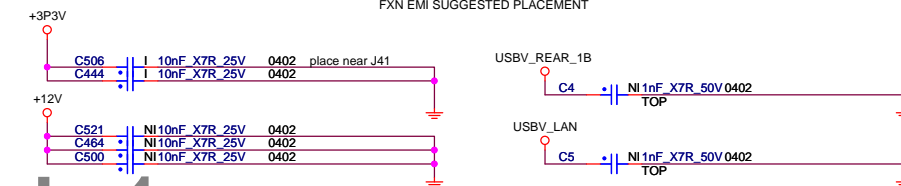
EMI CAP

FXN EMI SUGGESTED PLACEMENT

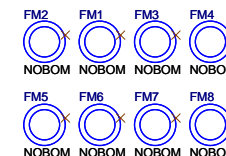
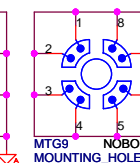
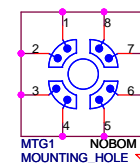
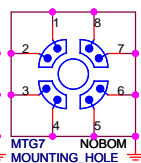
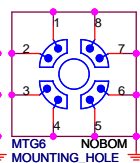
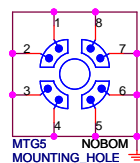
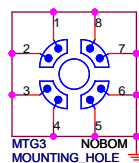
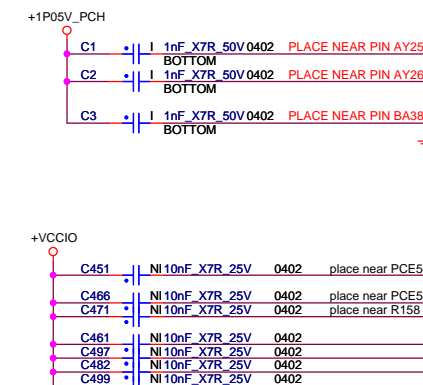


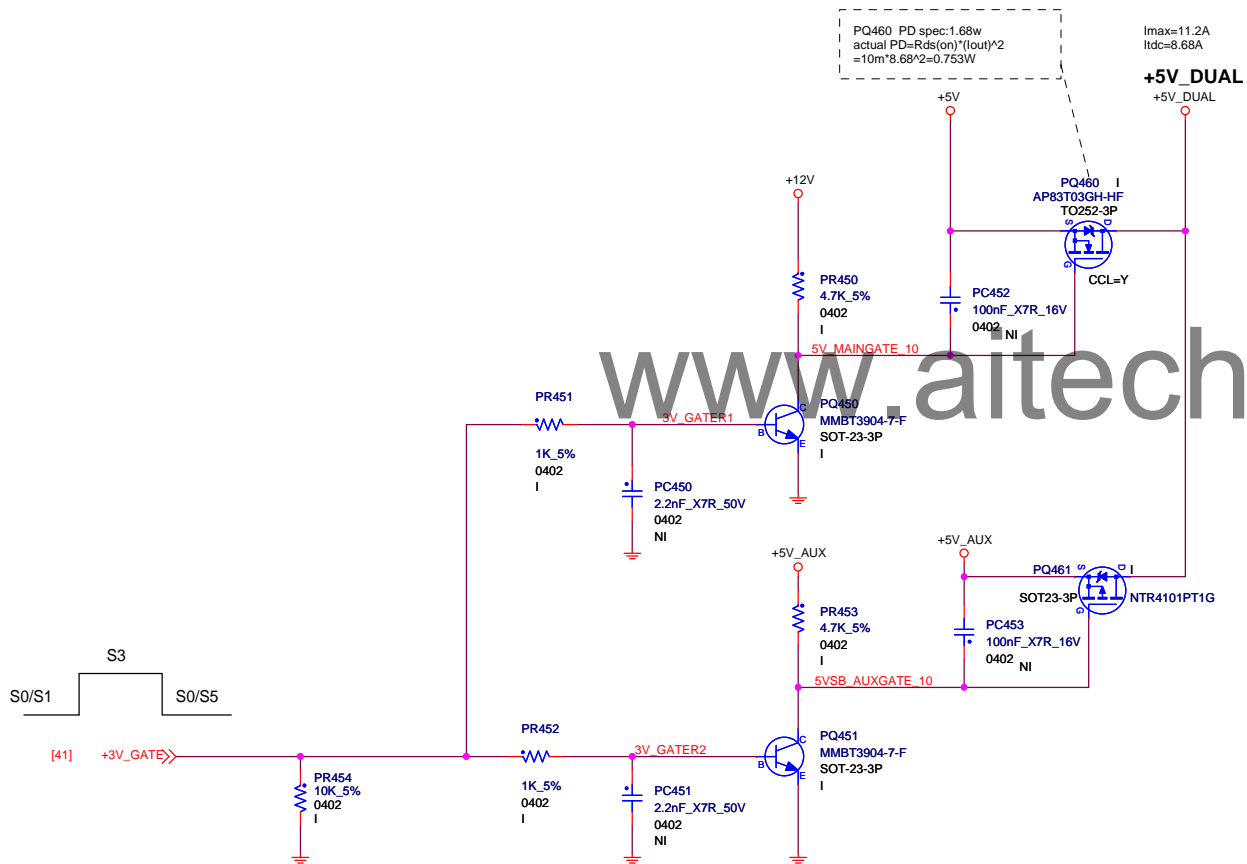
EMI CAP

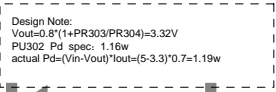
FXN EMI SUGGESTED PLACEMENT

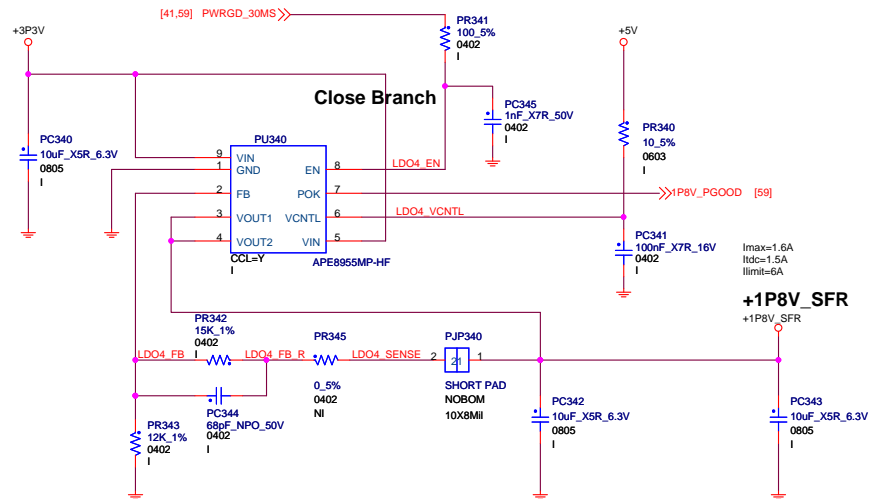


Decoupling caps for USB EMC issue

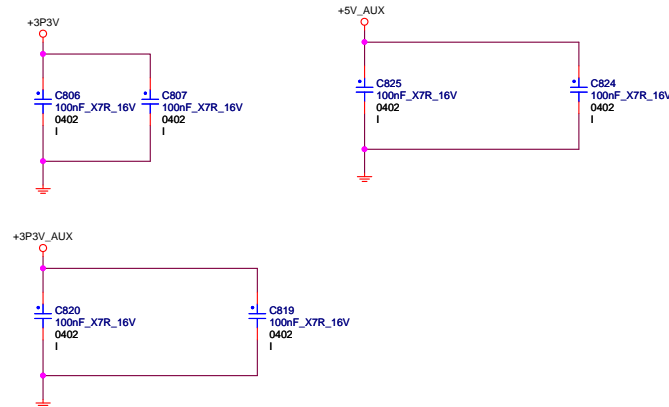






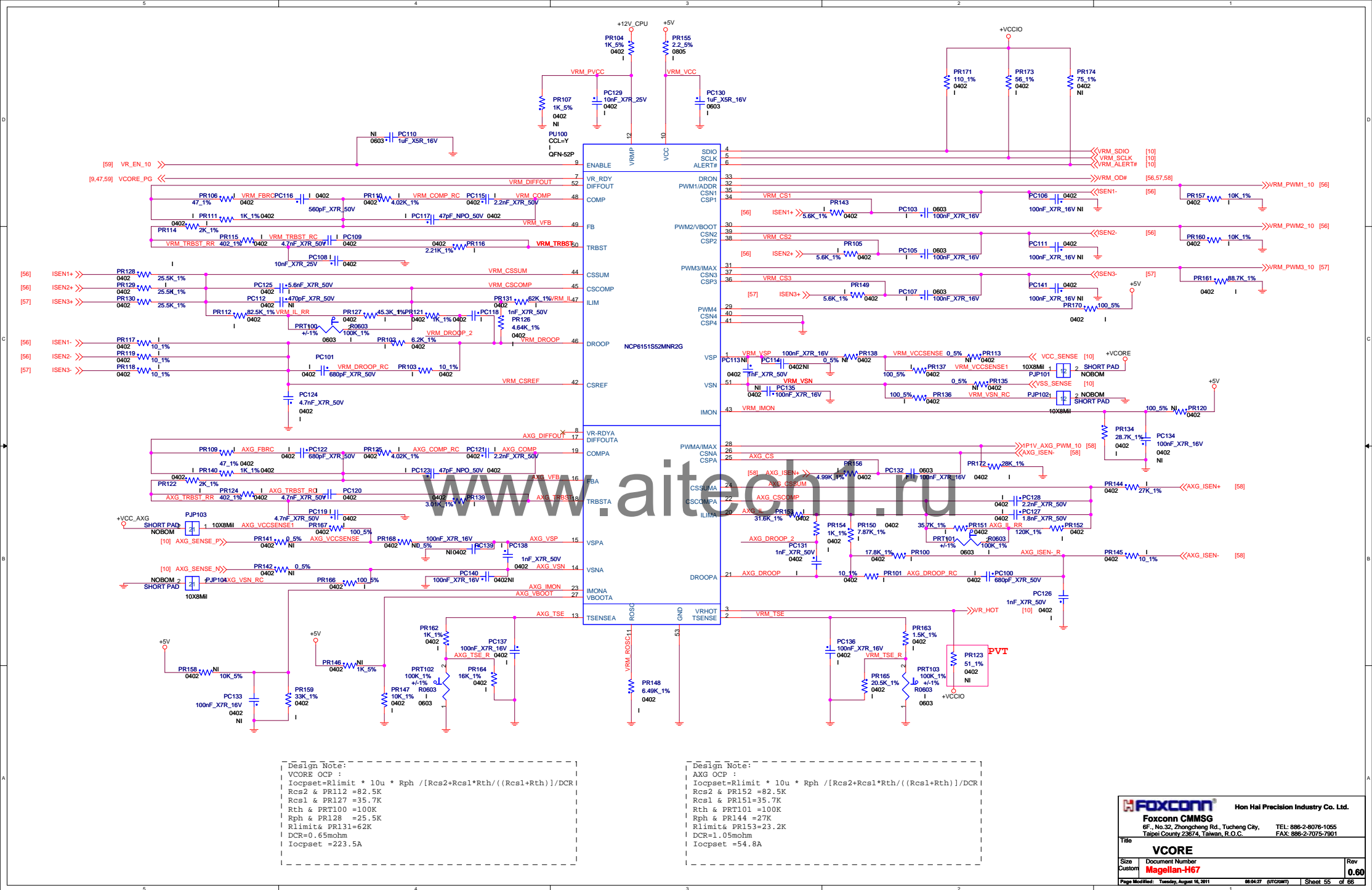


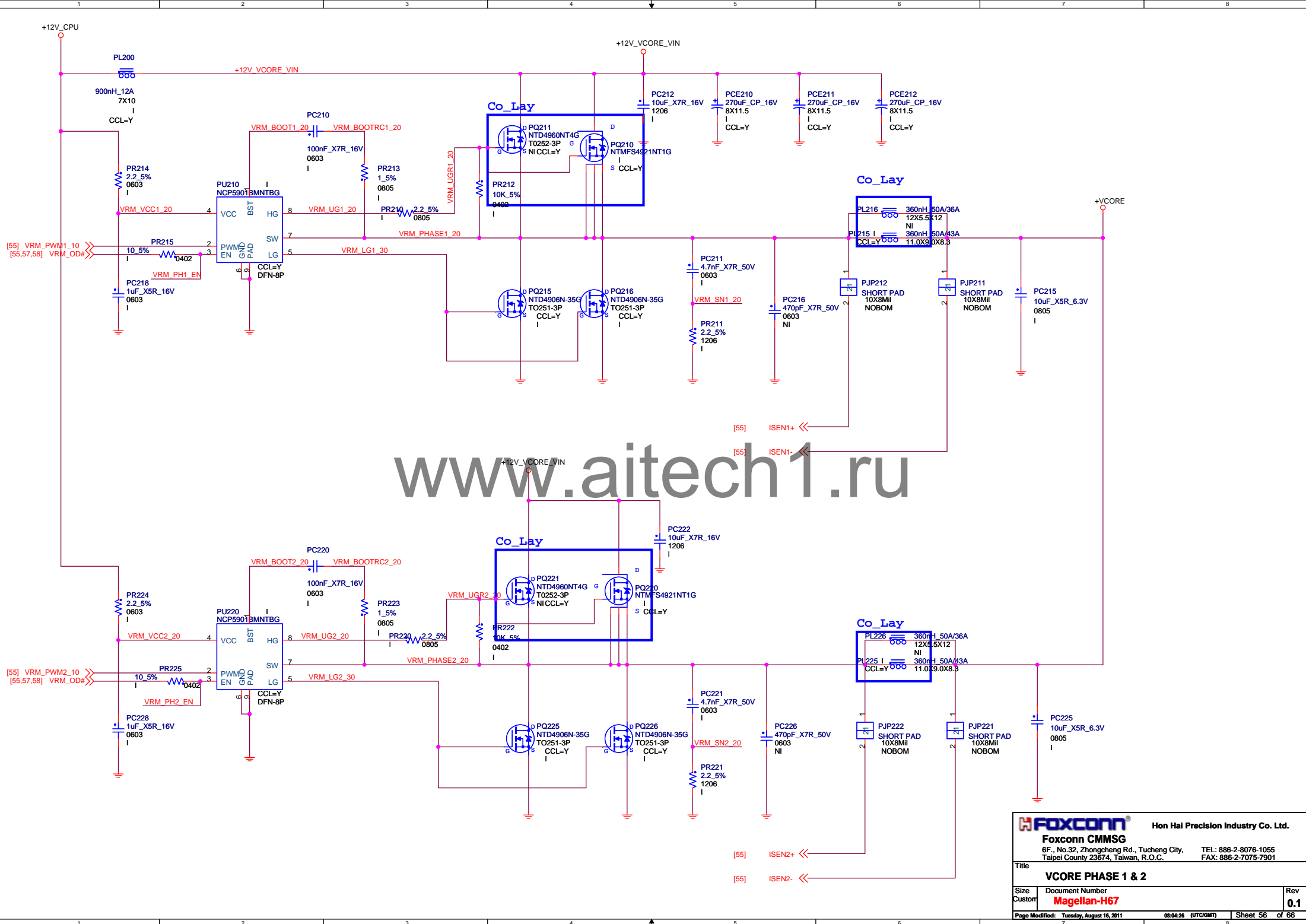
Design Note:
 Vout=0.8*(1+PR342/PR343)=1.8V
 PUS40 Pd spec: 3w
 actual Pd=(Vin-Vout)*Iout=(3.3-1.8)*1.5=2.25w



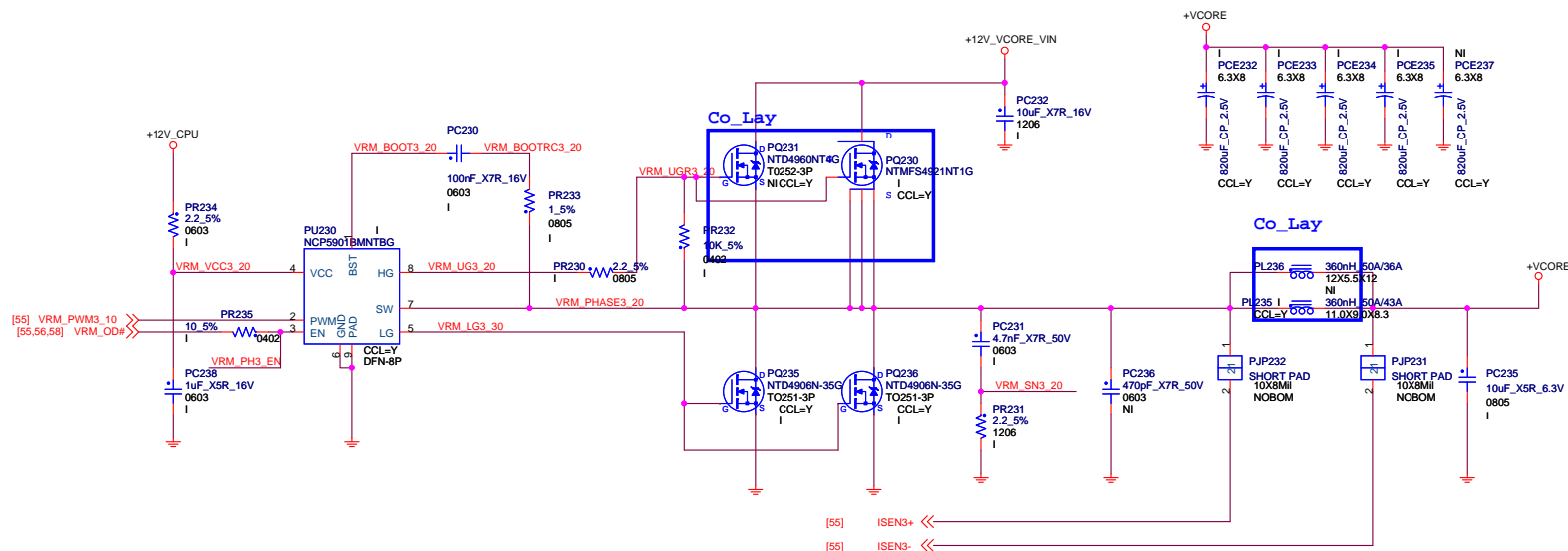
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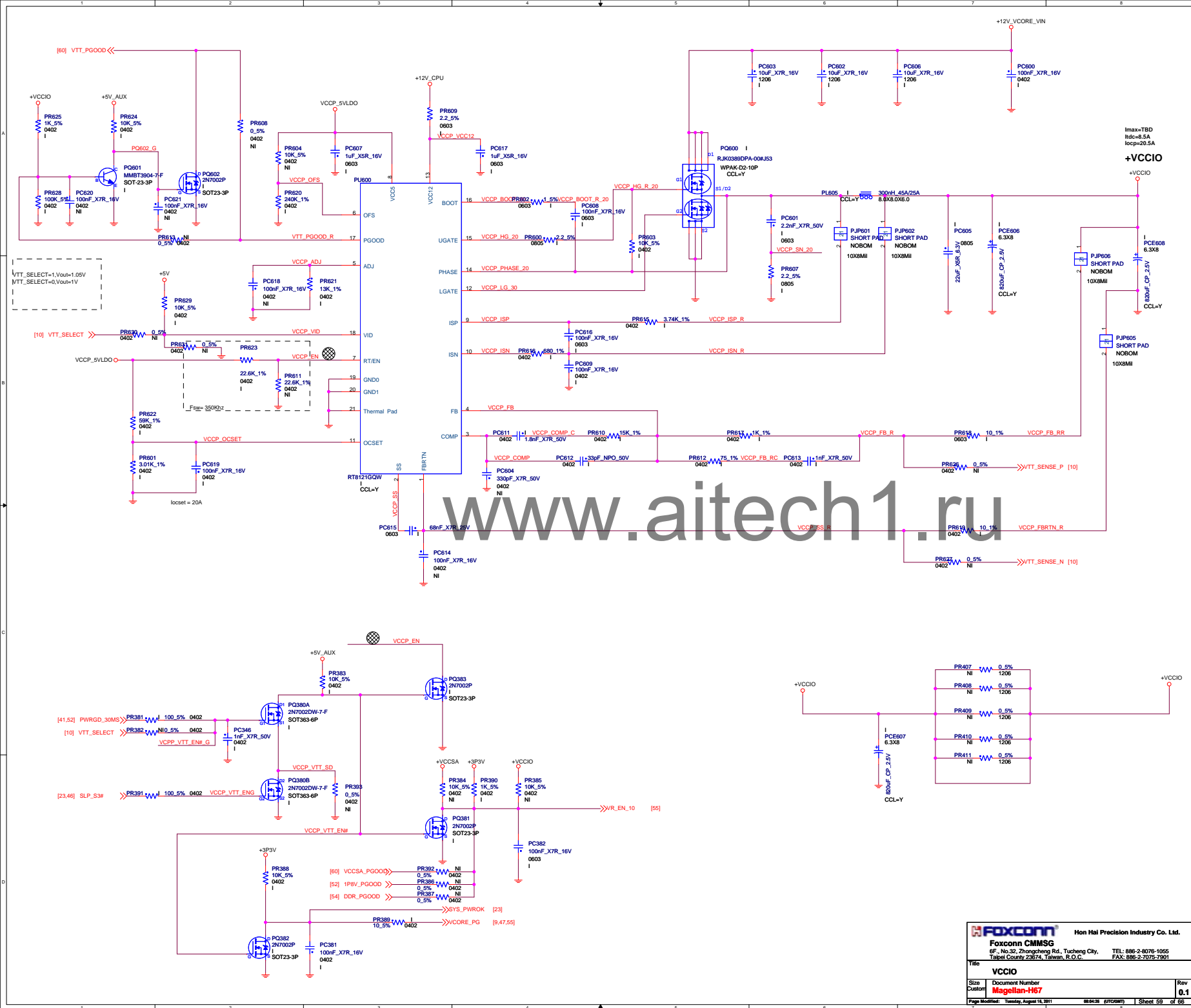


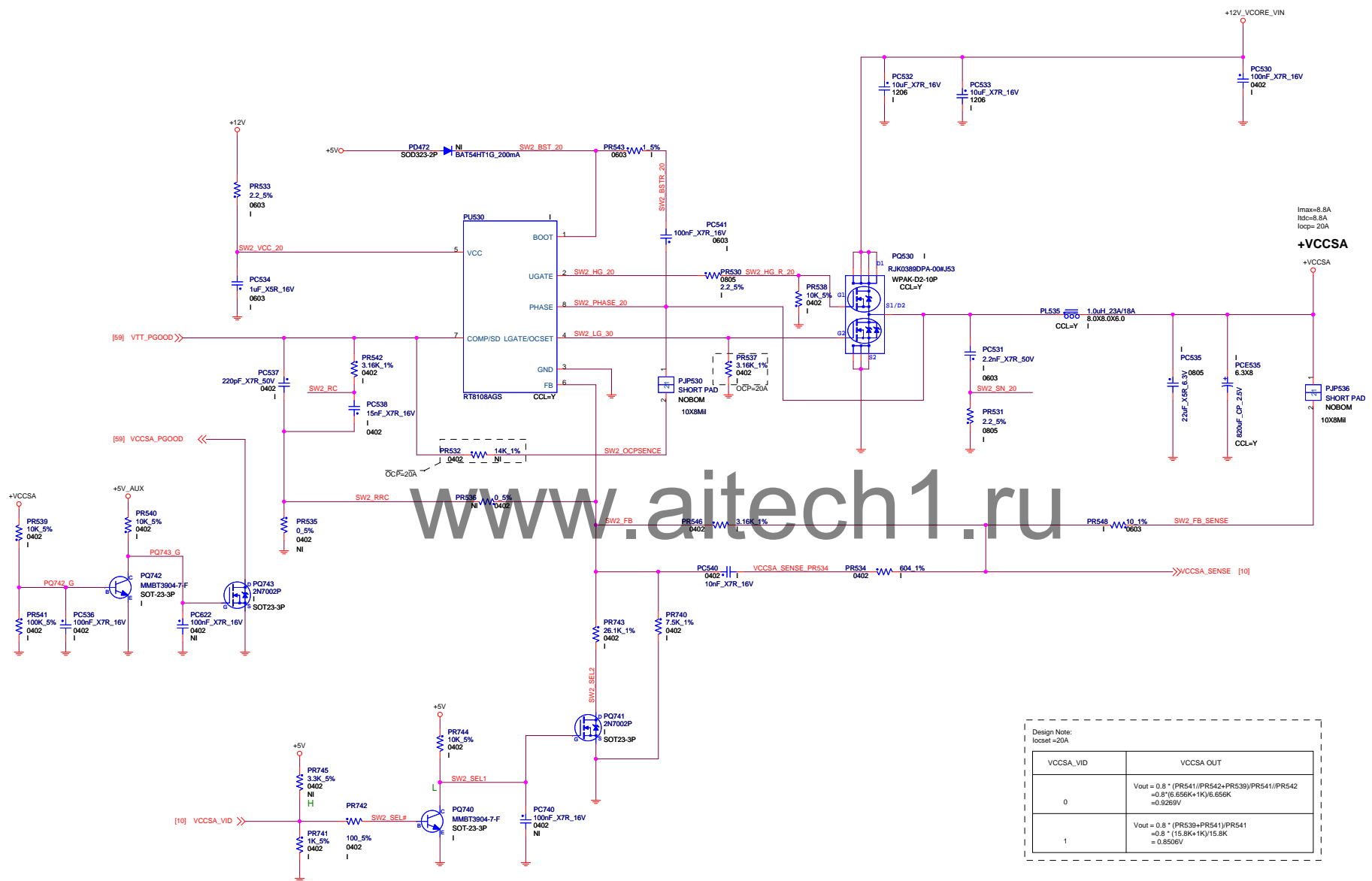
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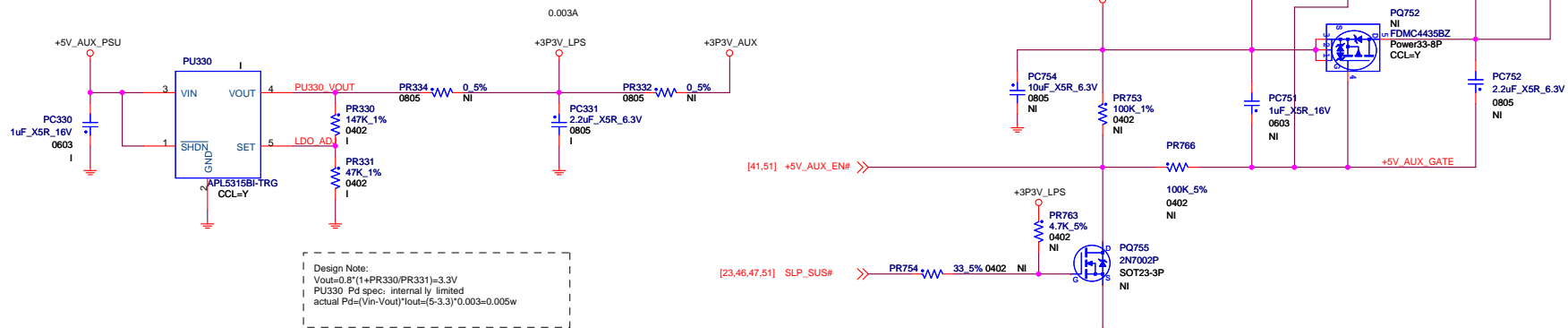
FOXCONN		Hon Hai Precision Industry Co. Ltd.	
Foxconn CMMSG			
6F, No.32, Zhongcheng Rd., Tucheng City, Taipei County 23674, Taiwan, R.O.C.		TEL: 886-2-8076-1055 FAX: 886-2-7075-7901	
Title VCORE PHASE 3			
Size Custom	Document Number Magellan-H67		R0.1
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Design Note:
I_{ocset} = 20A

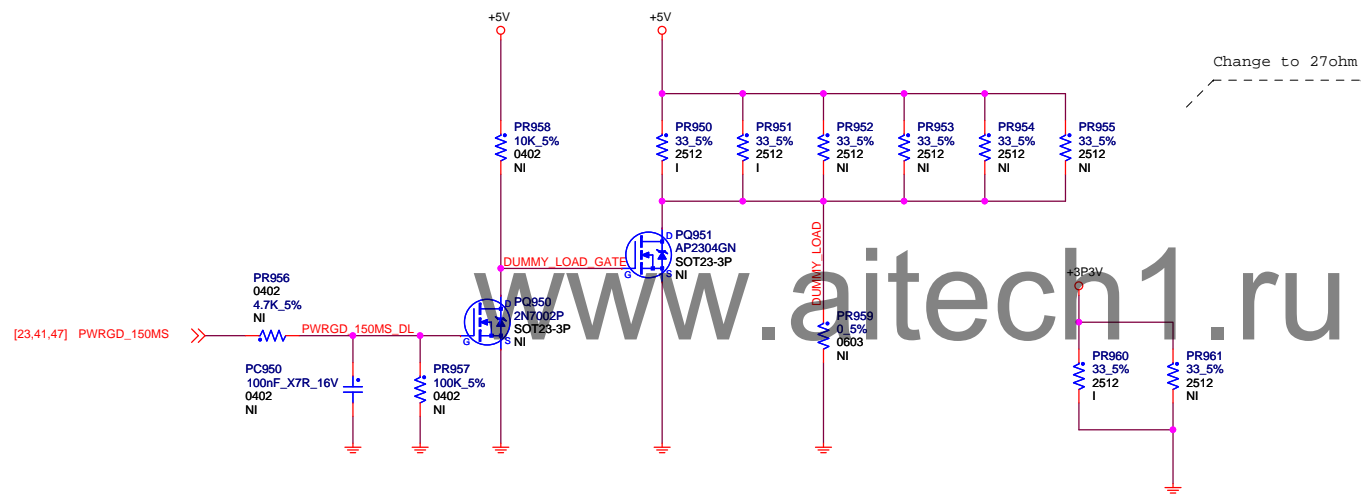
VCCSA_VID	VCCSA OUT
0	V _{out} = 0.8 * (PR541/(PR542+PR539))/PR541/PR542 = 0.8 * (15.856K+1K)/6.656K = 0.9266V
1	V _{out} = 0.8 * (PR539+PR541)/PR541 = 0.8 * (15.8K+1K)/15.8K = 0.8506V




Find cost down PN for PQ752 since Aux current is 2A max

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DUMMY LOAD



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Title Dummy Load			
Size A3	Document Number Magellan-H67		Rev 0.1
Page Modified: Tuesday, August 16, 2011		08:34:28 (UTC+08:00)	Sheet 62 of 66

PCH GPIO Information

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO0 BMBUSY#	Core	3.3V	IO	GPI	BMBUSY#	Pull up 10K to +3P3V.
GPIO1 TACH1	Core	3.3V	IO	GPI	OT_RECRY#	Pull up 10K to +3P3V.
GPIO2 PIRQE#	Core	5V	IOD	GPI	Non-Using	Pull up 8.2K to +3P3V.
GPIO3 PIRQF#	Core	5V	IOD	GPI	Non-Using	Pull up 8.2K to +3P3V.
GPIO4 PIRQ#	Core	5V	IOD	GPI	Non-Using	Pull up 8.2K to +3P3V.
GPIO5 PIRQH#	Core	5V	IOD	GPI	Non-Using	Pull up 8.2K to +3P3V.
GPIO6 TACH2	Core	3.3V	IO	GPI	LPC_SMI#	Pull up 10K to +3P3V.
GPIO7 TACH3	Core	3.3V	IO	GPI	COMM_B_DETECT#	Pull up 10K to +3P3V.
GPIO8	Suspend	3.3V	IO	GPO	Non-Using	Pull down 1K to GND.(Reserved)
GPIO9 OC5#	Suspend	3.3V	IO	Native	USB_OC2_BACK#_LAN	Connect to USB OC circuit Note11
GPIO10 OC6#	Suspend	3.3V	IO	Native	USB_OC0_BACK#_1	Connect to USB OC circuit Note11
GPIO11 SMBALERT#	Suspend	3.3V	IO	Native	SIO_PME#	Pull up 10K to +3P3V_AUX Note11
GPIO12 LAN_PHY_PWR_CTRL	Suspend	3.3V	IO	Native	Non-Using	Pull up 10K to +3.3V_LAN Option 10K pull down
GPIO13	Suspend	3.3V	IO	GPI	FWH_WP#_PCH reserve	Pull up 10K to +3P3V_AUX, notice (R343) Note4
GPIO14 OC7#	Suspend	3.3V	IO	Native	USB_OC1_BACK#_2	Connect to USB OC circuit
GPIO15	Suspend	3.3V	IO	GPO	PCH_OBSFN_C0(PROTO)	Pull up 1K to +3P3V_AUX
GPIO16 SATA6P	Core	3.3V	IO	GPI	HOOD_SW_DET#	Pull up 10K to +3P3V.
GPIO17 TACH0	Core	3.3V	IO	GPI	LPT_DET#	Pull up 10K to +3P3V
GPIO19 SATA1GP	Core	3.3V	IO	GPI	Non-Using	Pull up 10K to +3P3V.10k Nl,need I
GPIO20 PCIECLKRQ2#	Core	3.3V	IO	Native	Non-Using	Pull up 10K to +3P3V
GPIO21 SATA0GP	Core	3.3V	IO	GPI	F_AUDIO_DET#	Pull up 10K to +3P3V.
GPIO22 SCLCK	Core	3.3V	IO	GPI	CLR_CMOS (Slowware)	Pull up 10K to +3P3V (For E4 Jumper)
GPIO23 LDR01#	Core	3.3V	IO	Native	Non-Using	NONE(Test Point)
GPIO24 MEM_LED	Suspend	3.3V	IO	GPO	SKTOCC#(Reserve)	Reserve 0ohm to SKTOCC#
GPIO27	Deep Sleep	3.3V	IO	GPI	Non-Using	Pull up 10K to +3P3V_LPS
GPIO28	Suspend	3.3V	IO	GPO	Non-Using	Pull down 1K to GND (Reversed)
GPIO29 SLP_LAN#	Suspend	3.3V	IO	GPI	Non-Using	Pull up 10K to +3P3V_AUX
GPIO30 SUSWARN#	Deep Sleep	3.3V	IO	Native	SUS_WARN# Reserve	Pull up 10K to +3P3V_AUX(should I) Pull down 1K to GND(Reserved)
GPIO31	Deep Sleep	3.3V	IO	GPI	Non-Using	Pull up 10K to +3P3V_LPS Note 6
GPIO32	Core	3.3V	IO	GPO	Test pin	best to add pull up 10K to +3P3V Note4
GPIO33	Core	3.3V	IO	GPO	Non-Using	Pull up 10K to +3P3V Note4
GPIO34 STP_PC1#	Core	3.3V	IO	GPI	FRONT_USB_DET#_1	Pull up 10K to +3P3V

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO35	Core	3.3V	IO	GPO	LAN_DISABLE#	Pull down 1K to +3P3V,15Kto GND
GPIO36 SATA2GP	Core	3.3V	IO	GPI	BRD_REV0	Pull up 200K to +3P3V.
GPIO37 SATA3GP	Core	3.3V	IO	GPI	BRD_REV1	Pull up 200K to +3P3V.
GPIO38 SLOAD	Core	3.3V	IO	GPI	FRONT_USB_DET#_4	Pull up 10K to +3P3V
GPIO39 SDATAOUT0	Core	3.3V	IO	GPI	BRD_ID0	Pull down 10K to GND Option pull up 10K to +3P3V.
GPIO40 OC1#	Suspend	3.3V	IO	Native	USB_OC2_FRONT#2	Connect to USB OC circuit
GPIO41 OC2#	Suspend	3.3V	IO	Native	Non-Using	Pull up 10K to +3P3V_AUX.
GPIO42 OC3#	Suspend	3.3V	IO	Native	Non-Using	Pull up 10K to +3P3V_AUX.
GPIO43 OC4#	Suspend	3.3V	IO	Native	CLR_PSWD#	Pull up 10K to +3P3V_AUX.
GPIO44 PCIECLKRQ5#	Suspend	3.3V	IO	Native	Non-Using	Pull up 10K to +3P3V_AUX
GPIO45 PCIECLKRQ6#	Suspend	3.3V	IO	Native	Non-Using	Pull up 10K to +3P3V_AUX
GPIO46 PCIECLKRQ7#	Suspend	3.3V	IO	Native	Non-Using	Pull up 10K to +3P3V_AUX
GPIO48 SDATAOUT1	Core	3.3V	IO	GPI	TCM_DIS#	Pull up 10K to +3P3V
GPIO49 SATA5GP TEMP_ALERT#	Core	3.3V	IO	GPI	BRD_ID1	Pull up 10K to +3P3V Pull down 10K to GND(option)
GPIO50 REQ1#	Core	5.0 V	IO	Native	Non-Using	Pull up 10K to +3P3V. Note11
GPIO51 GNT1#	Core	3.3V	IO	Native	Non-Using	None
GPIO52 REQ2#	Core	5.0V	IO	Native	Non-Using	Pull up 10K to +3P3V
GPIO53 GNT2#	Core	3.3V	IO	Native	Non-Using	Reserve 4.7K pull down to GND
GPIO54 REQ3#	Core	5.0 V	IO	Native	BOOT_BLOCK_EN	Pull up 10K to +3P3V, or Pull down 11k to GND
GPIO55 GNT3#	Core	3.3V	IO	Native	Non-Using	Reserve 4.7K pull down to GND
GPIO57	Suspend	3.3V	IO	GPI	Non-Using	Option pull up 10K to +3.3V_AUX Pull down 10K to GND
GPIO58 SML1CLK	Suspend	3.3V	IO	Native	SML1CLK	Pull up 2.2K to +3P3V_AUX
GPIO59 OC0#	Suspend	3.3V	IO	Native	USB_OC6_FRONT#1	Connect to USB OC circuit
GPIO60 SML0ALERT#	Suspend	3.3V	IO	Native	MONO_DIS#	Pull high 10K to +3P3V_AUX, check 3504 disable circuit
GPIO61 SUS_STAT#	Suspend	3.3V	IO	Native	TPM LPD_PD#	Reserved 0 ohm resistor
GPIO62 SUSCLK	Suspend	3.3V	IO	Native	test Point	none
GPIO63 SLP_S5#	Suspend	3.3V	IO	Native	SLP_S5#	None
GPIO64 CLKOUTFLEX0	Core	3.3V	IO	Native	Non-Using	NONE(Test Point)
GPIO65 CLKOUTFLEX1	Core	3.3V	IO	Native	Non-Using	NONE(Test Point)
GPIO66 CLKOUTFLEX2	Core	3.3V	IO	Native	Non-Using	NONE(Test Point)
GPIO67 CLKOUTFLEX3	Core	3.3V	IO	Native	CK_P_24M_SIO	NONE
GPIO68 TACH4	Core	3.3V	IO	GPI	FRONT_USB_DET#_2	Pull up 10K to +3P3V

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO69 TACH5	Core	3.3V	IO	GPI	BRD_REV2	Pull down 10K to GND Option pull up 10K to +3P3V.
GPIO70 TACH6	Core	3.3V	IO	Native	BOOTBLOCK_RECRY#	Pull up 10K to +3P3V Jumper pull low to GND(PROTO)
GPIO71 TACH7	Core	3.3V	IO	Native	FRONT_USB_DET#_3	Pull up 10K to +3P3V
GPIO72	Suspend	3.3V	IO	GPO	+3P3V_AUX_SW	Pull up 10K to +3P3V_AUX Note4
GPIO74 PCHHOT# SML1ALERT#	Suspend	3.3V	IO	Native	Non-Using	Pull up 2.2K to +3P3V_AUX Note11
GPIO75 SML1DATA	Suspend	3.3V	IO	Native	SML1DATA	Pull up 2.2K to +3P3V_AUX

Note4
The functionality that is multiplexed with the GPIO may not be utilized in desktop configuration.

Note6
In an Intel? ME disabled system, GPIO31 may be used as ACPRESENT from the EC.

Note8
For GPIOs where GPIO vs. Native Mode is configured via SPI Soft Strap, the corresponding GPIO_USE_SEL bits for these GPIOs have no effect. The GPIO_USE_SEL bits for these GPIOs may change to reflect the Soft-Strap configuration even though GPIO Lockdown Enable (GLE) bit is set.

Note10.
Once Soft-strap is set to GPIO mode, this pin will default to GP Input. When Soft-strap is SLP_LAN# usage and if Host BIOS does not configure as GP Output for SLP_LAN# control, SLP_LAN# behavior will be based on the setting of the RTC backed SLP_LAN# Default Bit (D31:F0:A4h:Bit 8).

Note11.
When the multiplexed GPIO is used as GPIO functionality, care should be taken to ensure the signal is stable in its inactive state of the native functionality, immediately after reset until it is initialized to GPIO functionality

Note12 :In Main Power Well,Can instead be used as SATA[3:2]GP. This pin defaults to GPI.
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.

SIO IT8728F GPIO Information

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO10 PCIRST3#	Suspend	3.3V	DIOD8 DOD8	PCIRST3#	SIO_PCIEX18_RST# SIO_PCIEX1_RST#_1	Pull up 10kohm to +3p3V.
GPIO11 PCIRST2#	Core	3.3V	DIOD8 DOD8	PCIRST2#	SIO_TCM_RST# SIO_GLAN_RST#	None
GPIO12 PCIRST1#	Core	3.3V	DIOD8 DOD8	PCIRST1#	SIO_PCIE_RST#_PCI	None
GPIO14 PCH_C1	Core	3.3V	DIOD8 DOD8	PCH_C1	Non-using	None
GPIO15 CIRTX2 PCIRSTN#	Core	3.3V	DIOD8 DOD8 DI	PCIRSTN#	LPC_RST# PLTRST_N_SIO	Pull up 10kohm to +3p3V.
GPIO16 GIRX2 FAN_CTL5	Core	3.3V	DIOD8 DOD8 DI	FAN_CTL5	Non-using	Pull up 0kohm to +3P3V.(reserved)
GPIO17 R12#	Core	3.3V	DIOD8 DI	R12#	B_R12_3V3_SIO	Pull up 8.2kohm to +3p3V.
GPIO20 CTS2#	Suspend	3.3V	DIOD8 DI	CTS2#	CTS2#	None
GPIO21 DCD2#	Suspend	3.3V	DIOD8 DI	DCD2#	DCD2#	None
GPIO22	Suspend	3.3V	DIOD8	GPIO22	SIO_GP22_YLWLED	Pull up 2.2K to +3P3V_AUX
GPIO23 CPU_PG	Suspend	3.3V	DIOD8 DOD8	CPU_PG	SIO_GP23_GRNLED	Pull up 2.2K to +3P3V_AUX
GPIO24 RTS2# FAN_TAC5	Suspend	3.3V	DIOD8 DOD8 DI	FAN_TAC5	RTS2#	None
GPIO25 DSR2# FAN_TAC4	Suspend	3.3V	DIOD8 DI	FAN_TAC4	DSR2#	None
GPIO26 SOUT2	Suspend	3.3V	DIOD8 DOD8	SOUT2#	TXD2	None
GPIO27 SIN2	Suspend	3.3V	DIOD8 DI	SIN2#	RXD2	None
GPIO30 ATXPG	Core	3.3V	DIOD8 DI	ATXPG	PWROK_PS_LS	Pull up 10K to +3P3V
GPIO31 CTS1#	Core	3.3V	DIOD8 DI	CTS1#	CTS1#	None
GPIO32 RI1#	Core	3.3V	DIOD8 DI	RI1#	ARI1#	None
GPIO33 DCD1#	Core	3.3V	DIOD8 DI	DCD1#	DCD1#	None
GPIO34 RSTCONIN	Core	3.3V	DIOD8 DI	RSTCONIN	Non-Using	None
GPIO35 RSTCONOUT	Core	3.3V	DIOD8 DOD8	RSTCONOUT	Non-Using	None
GPIO36 FAN_CTL3	Core	3.3V	DIOD8 DOD8	FAN_CTL3	Non-Using	None
GPIO37 FAN_TAC3	Core	3.3V	DIOD8 DI	FAN_TAC3	Non-Using	None
GPIO40 3VBSBW#	Suspend	3.3V	DIOD8 DOD8	3VBSBW#	3VBSBW#	None
GPIO41 SIN1	Suspend	3.3V	DIOD8 DI	SIN1	RXD1	None
GPIO42 PSON#	Suspend	3.3V	DIOD8 DOD8	PSON#	PSON#_SIO	None
GPIO43 PANSW#	Suspend	3.3V	DIOD8 DI	PANSW#	PWRBTN#_SIO	None
GPIO44 PWRON# JP8	Suspend	3.3V	DIOD8 DOD8 DI	PWRON#	PWRBTN_OUT#_SIO	None
GPIO45 DSR1#	Suspend	3.3V	DIOD8 DI	DSR1#	DSR1#	None
GPIO46 DSRB#	Unsupported	--				
GPIO47	Core	3.3 V	DIOD8	GPIO47	Non-Using	None

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO50	Core	3.3V	DIOD8	GPIO50	LPC_SM#	Pull up 10K to +3P3V
GPIO51 FAN_CTL2	Core	3.3V	DIOD8 DOD8	FAN_CTL2	SYS_FAN_PWM3	Pull up 4.7K to +3P3V
GPIO52 FAN_TAC2	Core	3.3V	DIOD8 DI	FAN_TAC2	SYS_FAN_TACH3	Pull up 10K to +3P3V
GPIO53 SUSC#	Suspend	3.3V	DIOD8 DI	SUSC#	SLP_S4#_SIO	None
GPIO54 PME#	Suspend	3.3V	DIOD8 DOD8	PME#	SIO_PME#	Pull up 10K to +3P3V_AUX
GPIO55 CIRR# RSMRST#	Suspend	3.3V	DIOD8 DI DOD8	RSMRST#	SIO_RSMRST#	Pull down 200k to GND.
GPIO56 MCLK	Core	3.3V	DIOD24 DIOD24	MCLK	MSCLK	Pull up 4.7K to +5V_DUAL
GPIO57 MDAT	Core	3.3V	DIOD24 DIOD24	MDAT	MSDATA	Pull up 4.7K to +5V_DUAL
GPIO60 KCLK	Core	3.3V	DIOD24 DIOD24	KCLK	KBDCLK	Pull up 4.7K to +5V_DUAL
GPIO61 KDAT	Core	3.3V	DIOD24 DIOD24	KDAT	KBDATA	Pull up 4.7K to +5V_DUAL
GPIO62 KRST#	Core	3.3V	DIOD8 DOD8	KRST#	KBRST#	Pull up 1K to +3P3V
GPIO63	Core	3.3V	DIOD8	GPIO63	Non-Using	None
GPIO64	Core	3.3V	DIOD8	GPIO64	Non-Using	None
GPIO65 PCH_D0 VLDT_EN	Core	3.3V	DIOD8 DOD8 DOD8	VLDT_EN	SML1DATA	Pull up 2.2K to +3P3V_AUX
GPIO66	Core	3.3V	DIOD8	GPIO66	Non-Using	None
GPIO67	Core	3.3V	DIOD8	GPIO67	Non-Using	None
GPIO70 PD0	Suspend	3.3V	DIOD24 DIOD24	PD0	XPB0	None
GPIO71 PD1	Suspend	3.3V	DIOD24 DIOD24	PD1	XPB1	None
GPIO72 PD2 BUSS10	Suspend	3.3V	DIOD24 DI	BUSS10	XPB2	None
GPIO73 PD3 BUSS11	Suspend	3.3V	DIOD24 DI	BUSS11	XPB3	None
GPIO74 PD4 BUSS12	Suspend	3.3V	DIOD24 DI	BUSS12	XPB4	None
GPIO75 PD5 BUSS00	Suspend	3.3V	DIOD24 DI DOD24	BUSS00	XPB5	None
GPIO76 PD6 BUSS01	Suspend	3.3V	DIOD24 DI DOD24	BUSS01	XPB6	None
GPIO77 PD7 BUSS02	Suspend	3.3V	DIOD24 DI DOD24	BUSS02	XPB7	None
GPIO80 SLCT	Suspend	3.3V	DIOD8 DI	SLCT#	SLCT	None
GPIO81 PE	Suspend	3.3V	DIOD8 DI	PE#	PE	None
GPIO82 BUSY	Suspend	3.3V	DIOD8 DI	BUSY#	BUSY	None
GPIO83 ACK#	Suspend	3.3V	DIOD8 DI	ACK#	ACK#	None
GPIO84 SLIN# SMBD_R1	Suspend	3.3V	DIOD24 DIO24 IO_SW	SMBD_R	XSIN#	None
GPIO85 INIT# SMBD_M1	Suspend	3.3V	DIOD24 DIO24 IO_SW	SMBD_M	XINIT#	None
GPIO86 AFD# SMBD_R1	Suspend	3.3V	DIOD24 DIO24 IO_SW	SMBD_R	XAFD#	None
GPIO87 STB# SMBD_M1	Suspend	3.3V	DIOD24 DI IO_SW	SMBD_M	XSTB#	None

IO Cell:
 D08:8mA Digital Output buffer
 D08:8mA Digital Open-Drain Output buffer
 D016:16mA Digital Output buffer
 D024:24mA Digital Output buffer
 D024L:24mA shink/8mA drive Digital Output buffer
 D108:8mA Digital Input/Output buffer
 D108:8mA Digital Open-Drain Input/Output buffer
 D1016:16mA Digital Input/Output buffer
 D1024:16mA Digital Open-Drain Input/Output buffer
 D1024:24mA Digital Input/Output buffer
 D1024:24mA Digital Open-Drain Input/Output buffer
 DI:Digital Input
 AI:Analog Input
 AO:Analog Output
 SST:Special design for SST interface
 PRC1:Special design for PRC1 interface
 IO_SW:Special type of Input/Output;pins of this type connected in pairs through a switch

PCH Strapping Pins


Signal	Usage	When Sampled	Pull high Pull low	Comment															
SPKR	No Reboot	Rising edge of PWROK	Pull down	The signal has a weak internal pull-down. Note: The internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).															
INIT3_V#	Reserved	Rising edge of PWROK	Pull up	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts.NOTE: This signal should not be pulled low															
QNT7# / GPIO55	Top-Block Swap Override	Rising edge of PWROK	Pull up	The signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST#deasserts. If the signal is sampled low, thisindicates that the system is strapped to the "topblock swap" mode (Cougar Point inverts A16 for all cycles targeting BIOS space).The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without QNT7# being pulled down.															
INTVSMEN	Integrated 1.05 V VRM Enable / Disable	Always	Pull up	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high															
QNT1#/ GPIO51/ BBS1	Boot BIOS Strap bit 1 BBS1	Rising edge of PWROK	Pull up	This Signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts.This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <table><tr><td>Bit11</td><td>Bit 10</td><td>Boot BIOS Destination</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table> NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GBE LAN. NOTE: PCI Boot BIOS destination is not supported on Mobile	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																	
0	1	Reserved																	
1	0	PCI																	
1	1	SPI																	
0	0	LPC																	
SATA1GP/ GPIO19	Boot BIOS Strap bit 0 BBS0	Rising edge of PWROK	Pull up	This Signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts.This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <table><tr><td>Bit11</td><td>Bit 10</td><td>Boot BIOS Destination</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table> NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GBE LAN. NOTE: PCI Boot BIOS destination is not supported on Mobile	Bit11	Bit 10	Boot BIOS Destination	0	1	Reserved	1	0	PCI	1	1	SPI	0	0	LPC
Bit11	Bit 10	Boot BIOS Destination																	
0	1	Reserved																	
1	0	PCI																	
1	1	SPI																	
0	0	LPC																	
QNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Pull up	This Signal has a weak internal pull-up. NOTE: The internal pull-up is disabled afterPLTRST# deasserts.Tying this strap low configures DMI for ESICompatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.															
HDA_SDO	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of RSMRST#	Pull down EI jump to Pull up	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. NOTE: The weak internal pull-down is disabled after PLTRST# deasserts. NOTE: Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel® Management Engine after chipset bringup and disable runtime Intel ME features. This is a debug mode and must not be asserted aftermanufacturing/debug.															
DP_TV5	For future processor compatibility	Rising edge of PWROK	Pull up	Pull-Up: For future processor compatibility This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Pull up	This signal has a weak internal pull-up. NOTE: The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.															
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	Pull down	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.															
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Pull up	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality															
SDVO_CTRLDA TA	Port B Detected	Rising edge of PWROK	Pull down	When '1'- Port B is detected: When '0'- Port B is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															
DDPC_CTRLDA TA	Port C Detected	Rising edge of PWROK	Pull up	When '1'- Port C is detected: When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															
DDPD_CTRLDA TA	Port D Detected	Rising edge of PWROK	Pull down	When '1'- Port D is detected: When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.															

Signal	Usage	When Sampled	Pull high Pull low	Comment
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	Pull up	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	N/A	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	N/A	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.

SIO NCT6681D Strapping Pins

Signal	Usage	When Sampled	Pull High/Low	Description
Pin33 - Strap0 - SCKI#	SCKI# (SPI Interface)	TBD	Pull down 1K ± Rxx	Pull High: - XOR Tree Mode Enable. Pull Down: - SPI Interface Enable
Pin34 - Strap1 - SCKI	SCKI (SPI Interface)	TBD	Pull down 1K ± Rxx	Pull High: - PS2 Port Tri-State Enable and KBC Disable. Pull Down: - SPI Interface Enable

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Title

PCH/SIO Strapping Pins

Size C

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Change List

Change List From P2-H61 to P2-H67 V0.1

- 1.Follow H67 PCA SPEC Define: 4 DIMM,2 channel
 - Add CH8A DIMM1 (P17),and the corresponding CN6TR2LACLK signals
 - Add CH8B DIMM1 (P19),and the corresponding CN6TR2LACLK signals
- 2.Follow H67 PCA SPEC Define(Change SATA0_1 to SATA3_0
 - Change the P63 from 2.0 Conn(LD1807V-855MD) to 3.0 CONN(L818077-W50D-4H),color:white
 - Change the P62 from 2.0 Conn(LD1807V-855ZD) to 3.0 CONN(L818077-Z50D-4P),color:Dark Blue
- 3.Follow H67 PCA SPEC Define: add two rear USB ports
 - Change USBX2 (UB1112C-8P28-4P) to USBX4(UB11123-Q0D3-4P)
 - Add USB12,13 to USBX4 conn ,add a group power50C8 for it
- 4.Follow H67 PCA SPEC Define(TBD): add TCM header
 - Add Lenovo TCM header J3 for cost onlynn ,add a group power50C8 for it

Change List From V0.10 to V0.11

- 1.Follow CPC consumer PCA SPEC Define
 - Change the Clear CMOS Tact Switch to header &Jumper mode

Change List From V0.11 to V0.12

- 1.Follow +3.3V_AUX&+5V_AUX/+3.3V&+5V sequences(0.7V) requier
 - Change D31&D32 from BAT54C-7-F(VI=1.0v) to B130LAW-7-F(VI=0.7v)

Change List From V0.12 to V0.20

1. Change PRT102 PRT103 PR123 from NI to I, PR102 from 5.1K_1% to 6.2K_1%
2. Change PR165 from 10K_1% to 20.5K_1%,PR163 from 0_5% to 1.5K_1%
3. Change PR164 from 7.87K_1% to 16K_1%, PR162 from 0_5% to 1K_1%
4. Change PR123 from I to NI

Change List From V0.20 to V0.21

- 1.For Proto phase debug using,remove the solder mask footprint
 - Change the P7 footprint from HMS2X30CZ_NVB_NP to HMS2X30CZ
 - Change the P4 footprint from HMS2X30CZ_NVB_NP to HMS2X30CZ

Change List From V0.21 to V0.22

- 1.For Agile system requier combination same parts to same P/N, and link some CIS
 - Change S06 from MMBT3904_NL to MMBT3904-7-F
 - Change SD10 and D5 from BAT54A_NL to BAT54A-7-F
 - Update SIZ STD PN and modify it as CCL-Y
 - Change C338, C341, C856 and C879 from EKY-6R3ETD471MF111 to 6.3YXG470MCR6.3X11
 - Change C852, C864, C865, C866, C870, C871 from EMK212BJ106KG-T to GRM21BR60J106K
 - Change SD3, SD4 and SCR3 from MMSD4148T1G to 1N4148W-7-F
 - Change the AJ2 from JA33333-DA18-4F 30u to JA33331-F11P-4F GF

Change List From V0.22 to V0.30

- 1.Follow PDG requier,update the GPIO pull high or down states
 - Install R504 pull up to +3.3V
 - Change R651 from 100k to 10k
 - Install R335 pull up to +3P3V_AUX
 - Change R594/R568 from 10k to 200k,for strap requier
 - NI PCH_GPIO57 Pull down RES R109,I Pull high RES R421
 - 2.For some pin have reduplicate Pull high or Pull Low resistance
 - Del LPC_SMI# pull high resistance SR245,Keep down R409
 - Del SIO_PME# pull high resistance SR208,Keep down R115
 - Del SML1CLK pull high resistance SR165,Keep down R422
 - Del SML1DATA Pull high resistance SR166,Keep down R332
- 3.For Front Audio Conn GPIO Detection, maybe cause the noise and EMI to audio plane
 - Adding C652 at F_AUDIO_DET#,closed to AJ3
- 4.Adding GPIO.Strap information at P63,P64,P65

Change List From V0.30 to V0.31

- 1.For Rear USB port layout routing smoothly
 - Swap Port 13 to10,12 to 13,11 to 12,10 to 11
- 2.For PS/2 power bleed
 - Adding reserved R90 pull +5V_FUSED down to GND
- 3.Change ESD parts BAV99 D16,D17,D18,D19 from I to NI
- 4.Adding the CPU cover @XU1-Cover 012-1000-5377
- 5.Change the some ecap pin length from longer to shorter
 - PCE475,PCE476,PCE477,PCE232,PCE233,PCE234,PCE235,PCE236,PCE237,
 - PCE606,PCE607,PCE608,PCE635,PCE275,PCE276,PCE277,PCE278
 - from APSE2R5ELL821MF08S to APSE2R5ETD821MF08S
- 6.For SATA3.0 CONN CIS P/N wrong,correct it
 - Correct the P62 P/N from 4070GK00-600-G to 34070GK00-600-G
- 7.Change U16 P/N from IT8803E-DX to IT8803E-JX
- 8.Change D16/D17/D18/D19 from BAV99 to BAV99-7-F

Change List From V0.31 to V0.32

- 1.For TCM Function detail define unknow
 - Resever the PCH GPIO asTCM_DET#,TCM_DIS# function
- 2.Follow SIO 8728 datasheet, PCIRST3# power by +3VSB
 - Resever PCIRST3# Pull up to +3P3V , keep change to +3P3V_AUX
3. Update the SIO 8728 GPIO check list [P64]

Change List From V0.32 to V0.33

- 1.For avoding the "T" layout topology
 - Adding R57,R64,R42,R56 at P7/P4 SMBUS

Change List From V0.33 to V0.34

- 1.For RI# circuit maybe not be waked by com port
 - Del SR45,SD10,NI R327, Change SCR3 to BAT54C,D5 toB130LAW
- Adding the C926,915,C442,C472 caps for COM port power de-coupling and EMI

Change List From V0.34 to V0.35

- 1.For EMI suggestion,adding some reserve caps for Power
- 2.Adding four stitching cap for CK_P_33M_TCM_K_P_33M_LPC change layer and reference plane
- 3.Adding the R189 for TCM +5V power reserveer
- 4.Install SMLINK0 pull high resistance

Change List From V0.35 to V0.36

- 1.Update the Parts side property according to latest board file
- 2.Follow DVI Design guideline
 - Change the DPB_HPD_R pull up resistance R614 from NI to I
- 3.Follow PDG and popeye test fail at DMIPLL power
 - Change R430 from 10hm to 0ohm
- 4.Follow PDG Pull up define for GPIO30/17
 - Install GPIO30/17 Pull up resistance R576/R254
- 5.Change the LU3/LU4 P/N SLVU2-8.4T to SLVU2.8-4.TBT

Change List From DVT V0.35 to PVT V0.10

2011/07/05

- 1.Follow CPC spec.
 - Add disable PCI slot independently circuit for PCI1 and PCI2
- 2.For DRMPVWRGD &H_PWRGD have noise
 - Change layout from top to bottom
- 3.For LAN disable function
 - Reserve the 0ohm
- 4.Del GPIO19 connect to TCM trace
- 5.The COM2 ports maybe ring up the system abnormally
 - change the ring circuitry
- 6.For sus_warn# have nonmonotonic Rise edge
 - Del C173
- 7.Follow spec define
 - Modify the SATA reference from SATA1../SATA4 to SATA0../SATA3
- 8.Change the DIMM reference from DIMM1/DIMM3/DIMM2/DIMM4 to DIMM1/DIMM2/DIMM3/DIMM4
9. For BOM unification
 - Change PQ470 from IPD075N03L G to NTD4960NT4G,
 - Change PQ272 from BSC079N03LSC G to NTMF54921NT1G,
 - Change PQ475 and PQ476 from IPD060N03L G to NTD4906NT4G
- 10.For power stability
 - Change PCE211 from NI to I

Change List From V0.10 to V0.11

- 1.Follow RSMRST# FT test fail(rootcause have not found)
 - Del the S5 to G3 bleed off the RSMRST# circuit(del them can pass)
- 2.For the MONO-OUT POP noise issue
 - NI the MONO_DISABLE# Pull-up RES R102 , and BIOS will change GPIO60 states from S5/S3/S4 to S0
- 3.Follow MPT suggestion
 - Del one BMP(NI BM3)

Change List From PVT V0.12 to MVB V1.00

- 1.Change PCB information to MVB
- 2.Add soldermask at XDP debug port
- 3.Change R528/R517 BOM porperty from "Proto" to "I"
- 4.Change U19 package type from DIP to SMD
- 5.Change below 0ohm RES footprint from "R0402" to "R0402_SHORT_MVB" and BOM from "I" to "NOBOM"
AR12,AR13,AR16,AR19,AR22,LR19,PR113,PR135,PR138,PR141,PR142,PR168,
PR345,PR386,PR392,PR393,PR626,PR627,PR476,PR536,R77,R79,R88,RE58,
R660,R933,R934,R130,R325,R185,R186,R189,R228,R255,R337,R395,
R371,R419,R426,R430,R432,R438,R531,R535,R541,R668,R729,R939,R283,
R284,R286,R287,R305,R311,R322,R324,R329,R351,R353,R354,R355,R364,
R365,R414,R429,R652,R440,SR1,SR4,SR127,SR130,SR147,SR148,SR151,
SR152,SR184,SR185,SR223,SR272,SR366,SR669,SR708,SR711,SR776
6.Change below 0ohm RES footprint from "R0603" to "R0603_SHORT_MVB" and BOM from "I" to "NOBOM"
AR18,LR13,PR314,PR488,PR959,SR223

Change List From V1.00 to V1.01

- 2011/08/15 :
- change PQ271,PQ470 from NTD4960NT4G to IPD075N03L G;
 - change PQ270,PQ272 from NTMF54921NT1G to BSC079N03LSC G;
 - change PQ275,PQ276,PQ475,PQ476 from NTD4906NT4G to IPD060N03L G.



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